EM120R-GL&EM160R-GL
Hardware Design

LTE-A Module Series

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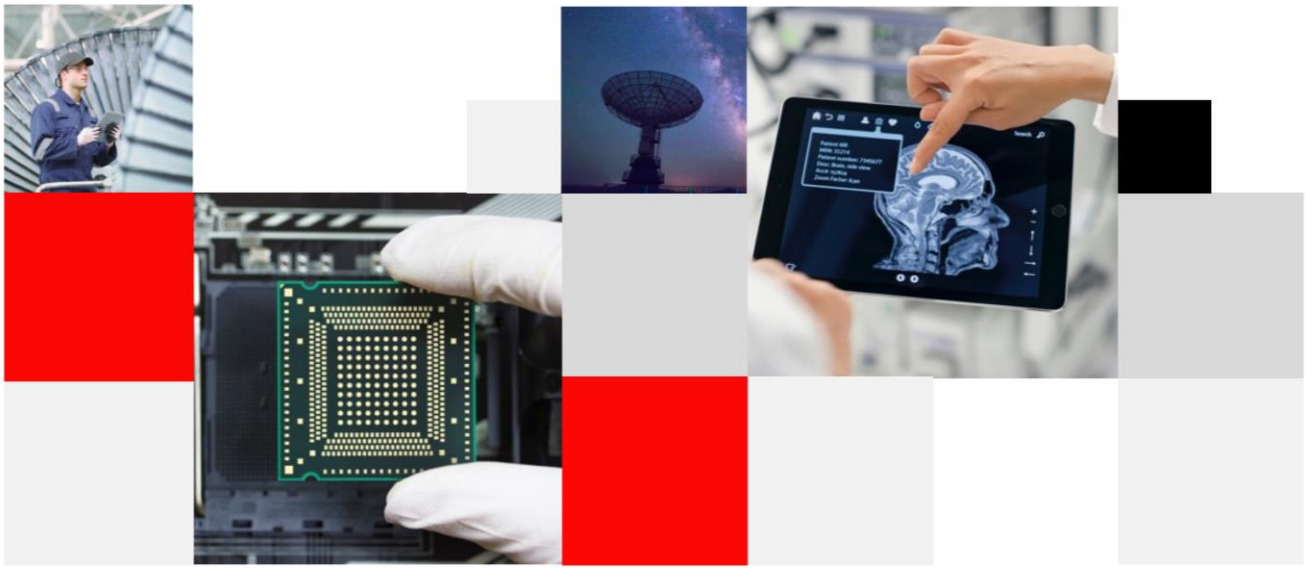

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2020-07-02	Jim HAN/ Lewis PENG	Creation of the document
1.0	2021-02-09	Jim HAN/ Davon ZHAO/ Lewis PENG	First official release
1.1	2021-03-18	Oscar LIU/ Lewis PENG	1. Added (U)SIM Hot-plug description (Chapter 4.1.2). 2. Added PCIe Power-on Timing Requirements of M.2 Specification (Chapter 4.3.3). 3. Added B29/32/46 dual-antenna conducted receiving sensitivity (Table 39). 4. Added B32 four-antenna conducted receiving sensitivity (Table 40).

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1 Introduction

1.1. Introduction

The hardware design defines EM120R-GL and EM160R-GL and describes the air and hardware interfaces which are connected to customers' applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of EM120R-GL and EM160R-GL. To facilitate its application in different fields, reference design is also provided for reference. Coupled with application notes and user guides, customers can use the module to design and set up mobile applications easily.

This document is applicable to the EM120R-GL and EM160R-GL modules.

1.2. Reference Standard

The module complies with the following standards:

- *PCI Express M.2 Specification Revision 2.0*, *Version 1.2*
- *PCI Express Base Specification Revision 2.0*
- *Universal Serial Bus Specification, Revision 3.0*
- *ISO/IEC 7816-3*
- *MIPI Alliance Specification for RF Front-End Control Interface version 2.0*
- *3GPP TS 27.007* and *3GPP* 27.005
- *3GPP TS 34.121-1*
- *3GPP TS 36.521-1*

1.3. Special Marks

Table 1: Special Marks

Mark	Definition
*	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported, unless otherwise specified.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, ANTCTL [0:3] refers to all four ANTCTL pins, ANTCTL0, ANTCTL1, ANTCTL2, and ANTCTL3.

2 Product Concept

2.1. General Description

EM120R-GL and EM160R-GL are LTE-A/UMTS/HSPA+ wireless communication modules with receive diversity. They provide data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks. They are standard WWAN M.2 Key-B modules. For more details, see *PCI Express M.2 Specification Revision 2.0, Version 1.2*.

EM120R-GL and EM160R-GL are industrial-grade modules for industrial and commercial applications only.

They support embedded operating systems such as Windows, Linux and Android, and also provide GNSS [1)] and voice functionality [2)] to meet specific application demands.

The following table shows the frequency bands and GNSS types of the module.

Table 2: Frequency Bands and GNSS Types of EM120R-GL&EM160R-GL

Mode	Frequency Bands
LTE-FDD (with Rx-diversity/MIMO [3)])	B1 [4)]/B2 [4)]/B3 [4)]/B4 [4)]/B5/B7 [4)]/ B8/B12/B13/B14/B17 [5)]/ B18/B19/B20/B25 [4)]/B26/B28/B29 [6)]/B30 [4)]/B32 [4) 6)]/B66 [4)]
LTE-TDD (with Rx-diversity/MIMO [3)])	B38 [4)]/B39 [4)]/B40 [4)]/B41 [4)]/B42/B43/B46 [6)]/B48
WCDMA (with Rx-diversity)	B1/B2/B3/B4/B5/B6/B8/B19
GNSS [1)]	GPS; GLONASS; BeiDou/COMPASS; Galileo

NOTES

1. [1)] GNSS function is optional.
2. [2)] EM120R-GL&EM160R-GL contain **Telematics** version and **Data-only** version. **Telematics**

version supports voice and data functions, while **Data-only** version only supports data function.
3. [3] 4 × 4 MIMO antennas only apply for EM160R-GL.
4. [4] EM160R-GL supports up to 4 × 4 MIMO in DL direction.
5. [5] B17 is supported through MFBI + B12.
6. [6] LTE-FDD B29/B32 and LTE-TDD B46 support Rx only and are only for secondary component carrier.
7. For details about CA combinations, see ***document [1]***.

EM120R-GL and EM160R-GL can be applied in the following fields:

- Tablet PC and Laptop
- Remote Monitor System
- Wireless POS System
- Smart Metering System
- Wireless Router and Switch
- Other Wireless Terminal Devices

2.2. Key Features

Table 3: Key Features of EM120R-GL&EM160R-GL

Feature	Details
Function Interface	PCI Express M.2 Interface
Power Supply	● Supply voltage: 3.135–4.4 V ● Typical supply voltage: 3.7 V
(U)SIM Interface	● Compliant with *ISO/IEC 7816-3* ● Support (U)SIM card: 1.8/3.0 V ● Support Dual SIM Single Standby
USB Interface	● Compliant with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0. ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output, and voice over USB*. ● Support USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6–5.10, Android 4.x/5.x/6.x/7.x/8.x/9.x/10.x
PCIe Interface	● Complaint with PCIe Gen 2 ● PCIe × 1, supporting 5 Gbps per lane ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output.

PCM Interface*	● Used for audio function with external codec ● Support 16-bit linear data format ● Support long and short frame synchronization ● Support master and slave modes, but must be the master in long frame synchronization
Rx-diversity	● LTE/WCDMA
Antenna Interfaces	**EM160R-GL** ● Main, Rx-diversity/GNSS, MIMO1 and MIMO2 antenna connectors ● 50 Ω impedance. **EM120R-GL** ● Main and Rx-diversity/GNSS antenna connectors ● 50 Ω impedance.
Transmitting Power	**PCIe Interface** ● WCDMA Bands: Class 3 (24 dBm +1/-3 dB) ● LTE-FDD - B30: Class 3 (22 dBm +1/-2 dB) - Other Bands: Class 3 (24 dBm +1/-2 dB) ● LTE-TDD - B41: Class 3 (23 dBm +1/-2 dB) - B42/B43/B48: Class 3 (21 dBm +1/-2 dB) - B41 HPUE: Class 2 (25.5 dBm +1/-2 dB) - Other Bands: Class 3 (24 dBm +1/-2 dB) **USB Interface** ● WCDMA Bands: Class 3 (24 dBm +1/-3 dB) ● LTE-FDD Bands: Class 3 (23 dBm ±2 dB) ● LTE-TDD - B41 HPUE: Class 2 (25.5 dBm +1/-2 dB) - Other Bands: Class 3 (23 dBm ±2 dB)
LTE Features	**EM160R-GL** ● Up to LTE Cat 16 ● 1.4–100 MHz (5CA) RF bandwidth ● Support 4 × 4 MIMO in DL direction ● Support uplink QPSK, 16QAM and 64QAM modulation ● Support downlink QPSK, 16QAM and 64QAM and 256QAM modulation ● Data rate: up to 1000 Mbps (DL)/150 Mbps (UL) **EM120R-GL** ● Up to LTE Cat 12 ● 1.4–60 MHz (3CA) RF bandwidth ● Support 2 × 2 MIMO in DL direction ● Support uplink QPSK, 16QAM and 64QAM modulation ● Support downlink QPSK, 16QAM and 64QAM and 256QAM modulation ● Data rate: up to 600 Mbps (DL)/150 Mbps (UL)
UMTS Features	● 3GPP R9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA

	● Support QPSK, 16QAM and 64QAM modulation ● Data rate: - DC-HSDPA: max. 42 Mbps (DL) - HSUPA: max. 5.76 Mbps (UL) - WCDMA: max. 384 kbps (DL)/384 kbps (UL)
GNSS Features	● Qualcomm Gen9-VT ● Support GPS, GLONASS, BeiDou/COMPASS and Galileo ● Protocol: NMEA 0183 ● Data update rate: 1 Hz
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Internet Protocol Features	QMI/MBIM/NITZ/PING/HTTP/HTTPS protocols
Firmware Upgrade	USB 2.0 interface, PCIe interface and DFOTA
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
Physical Characteristics	● M.2 Key-B ● Size: (30.0 ±0.15) mm × (42.0 ±0.15) mm × (2.3 ±0.2) mm ● Weight: approx. 6.8 g
Temperature Range	● Operating temperature range: -25 to +75 °C [1)] ● Extended temperature range: -40 to +85 °C [2)] ● Storage temperature range: -40 to +90 °C
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
2. [2)] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a functional diagram of EM120R-GL and EM160R-GL.

- Power management
- Baseband
- LPDDR4X SDRAM + NAND Flash
- Radio frequency
- M.2 Key-B interface

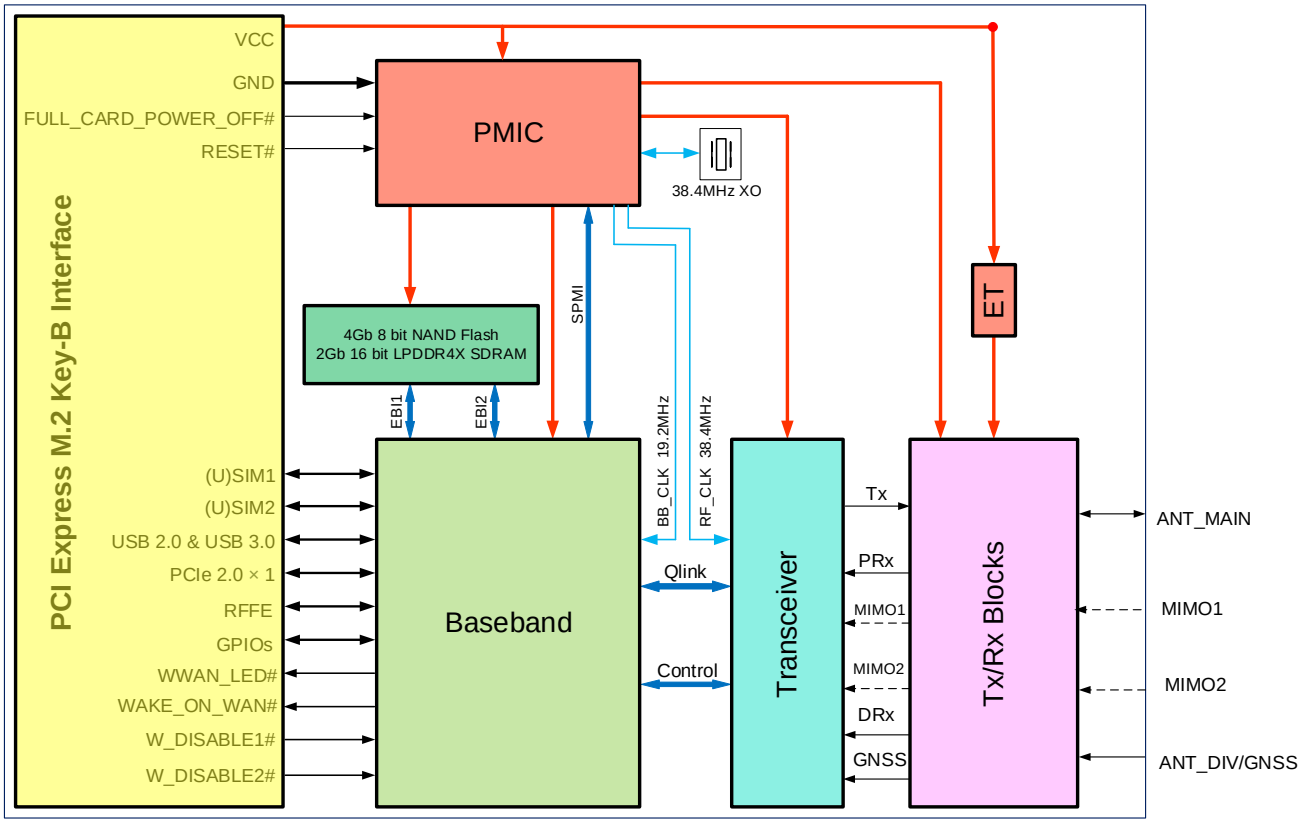


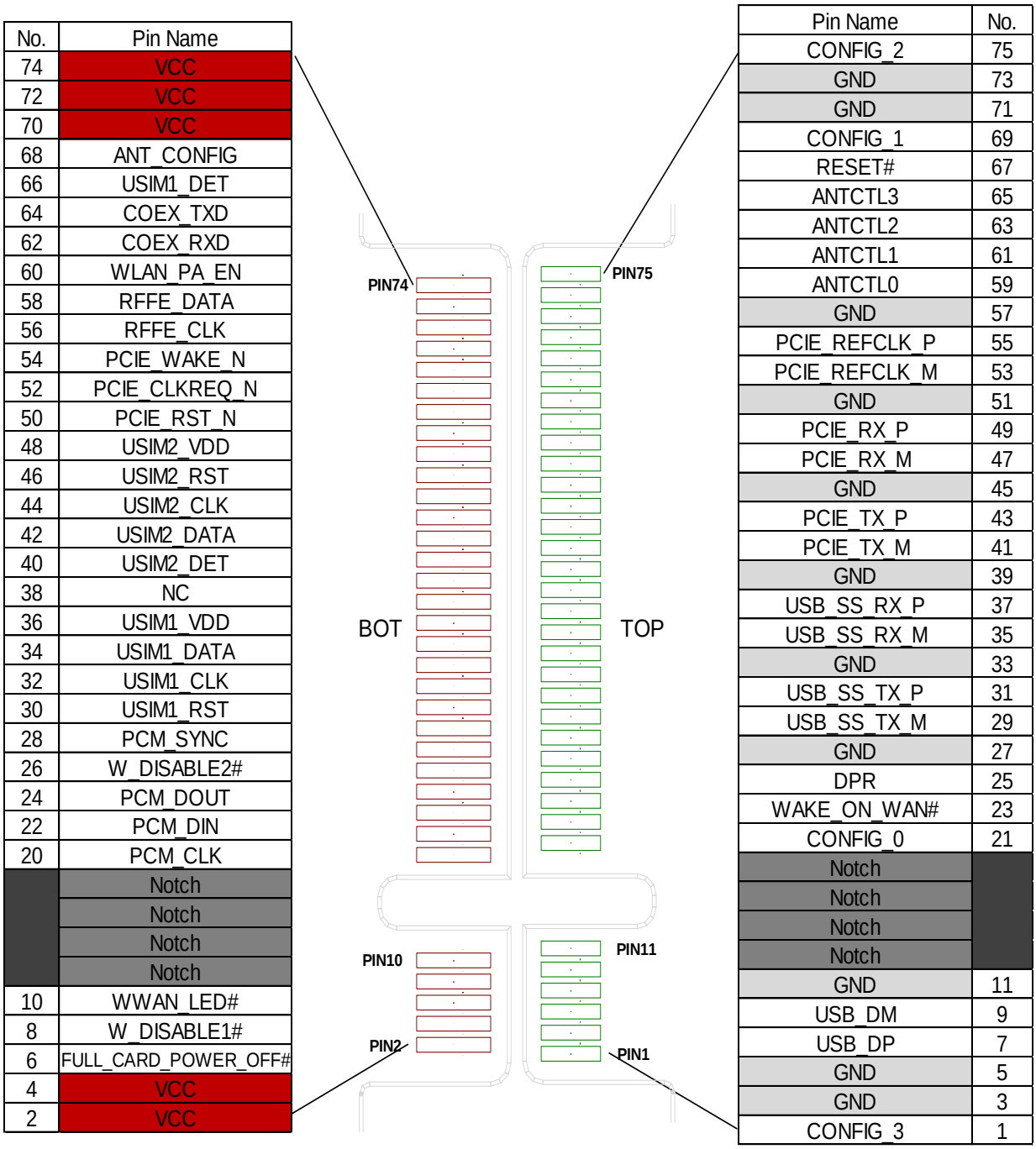
Figure 1: Functional Diagram

NOTE

MIMO1 and MIMO2 antennas are only applicable to the EM160R-GL module.

2.4. Pin Assignment

The following figure shows the pin assignment of the module. The top side contains module and antenna connectors.



No.	Pin Name
74	VCC
72	VCC
70	VCC
68	ANT_CONFIG
66	USIM1_DET
64	COEX_TXD
62	COEX_RXD
60	WLAN_PA_EN
58	RFFE_DATA
56	RFFE_CLK
54	PCIE_WAKE_N
52	PCIE_CLKREQ_N
50	PCIE_RST_N
48	USIM2_VDD
46	USIM2_RST
44	USIM2_CLK
42	USIM2_DATA
40	USIM2_DET
38	NC
36	USIM1_VDD
34	USIM1_DATA
32	USIM1_CLK
30	USIM1_RST
28	PCM_SYNC
26	W_DISABLE2#
24	PCM_DOUT
22	PCM_DIN
20	PCM_CLK
	Notch
	Notch
	Notch
	Notch
10	WWAN_LED#
8	W_DISABLE1#
6	FULL_CARD_POWER_OFF#
4	VCC
2	VCC

Pin Name	No.
CONFIG_2	75
GND	73
GND	71
CONFIG_1	69
RESET#	67
ANTCTL3	65
ANTCTL2	63
ANTCTL1	61
ANTCTL0	59
GND	57
PCIE_REFCLK_P	55
PCIE_REFCLK_M	53
GND	51
PCIE_RX_P	49
PCIE_RX_M	47
GND	45
PCIE_TX_P	43
PCIE_TX_M	41
GND	39
USB_SS_RX_P	37
USB_SS_RX_M	35
GND	33
USB_SS_TX_P	31
USB_SS_TX_M	29
GND	27
DPR	25
WAKE_ON_WAN#	23
CONFIG_0	21
Notch	
Notch	
Notch	
Notch	
GND	11
USB_DM	9
USB_DP	7
GND	5
GND	3
CONFIG_3	1

Figure 2: Pin Assignment

2.5. Pin Description

Table 4: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pull Up
PD	Pull Down

The following table shows the pin definition and description of the module.

Table 5: Pin Description

Pin No.	Pin Name	I/O	Description	DC Characteristic	Comment
1	CONFIG_3	DO	Not connected internally		
2	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
3	GND		Ground		
4	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	

5	GND		Ground		
6	FULL_CARD_ POWER_OFF#	DI, PD	Turn on/off the module. High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Internally pulled down with a 100 kΩ resistor.
7	USB_DP	AIO	USB differential data (+)		
8	W_DISABLE1#	DI, OD	Airplane mode control. Active LOW.	1.8/3.3 V	
9	USB_DM	AIO	USB differential data (-)		
10	WWAN_LED#	DO, OD	RF status indication LED. Active LOW.	VCC	
11	GND		Ground		
12	Notch		Notch		
13	Notch		Notch		
14	Notch		Notch		
15	Notch		Notch		
16	Notch		Notch		
17	Notch		Notch		
18	Notch		Notch		
19	Notch		Notch		
20	PCM_CLK*	DIO, PD	PCM clock	1.8 V	
21	CONFIG_0	DO	Not connected internally		
22	PCM_DIN*	DI, PD	PCM data input	1.8 V	
23	WAKE_ON_ WAN#*	DO, OD	Wake up the host. Active LOW.	1.8/3.3 V	
24	PCM_DOUT*	DO, PD	PCM data output	1.8 V	
25	DPR	DI, PU	Dynamic power reduction. High level by default.	1.8 V	
26	W_DISABLE2#	DI, OD	GNSS disable control. Active LOW.	1.8/3.3 V	

27	GND		Ground		
28	PCM_SYNC*	DIO, PD	PCM data frame sync	1.8 V	
29	USB_SS_TX_M	AO	USB 3.0 super-speed transmit (-)		
30	USIM1_RST	DO, PD	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V	
31	USB_SS_TX_P	AO	USB 3.0 super-speed transmit (+)		
32	USIM1_CLK	DO, PD	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V	
33	GND		Ground		
34	USIM1_DATA	DIO, PU	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V	
35	USB_SS_RX_M	AI	USB 3.0 super-speed receive (-)		
36	USIM1_VDD	PO	(U)SIM1 card power supply	1.8/3.0 V	
37	USB_SS_RX_P	AI	USB 3.0 super-speed receive (+)		
38	NC		NC		
39	GND		Ground		
40	USIM2_DET*	DI, PU	(U)SIM2 card hot-plug detect	1.8 V	Internally pulled up to 1.8 V [1)]
41	PCIE_TX_M	AO	PCIe transmit (-)		
42	USIM2_DATA	DIO, PU	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V	
43	PCIE_TX_P	AO	PCIe transmit (+)		
44	USIM2_CLK	DO, PD	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V	
45	GND		Ground		
46	USIM2_RST	DO, PD	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V	
47	PCIE_RX_M	AI	PCIe receive (-)		
48	USIM2_VDD	PO	(U)SIM2 card power supply	1.8/3.0 V	
49	PCIE_RX_P	AI	PCIe receive (+)		

50	PCIE_RST_N	DI, OD	PCIe reset. Active LOW.		
51	GND		Ground		
52	PCIE_CLKREQ_N	DO, OD	PCIe clock request. Active LOW.		
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)		
54	PCIE_WAKE_N	DO, OD	PCIe wake up. Active LOW.		
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)		
56	RFFE_CLK [2] *	DO, PD	Used for external MIPI IC control	1.8 V	
57	GND		Ground		
58	RFFE_DATA [2] *	DIO, PD	Used for external MIPI IC control	1.8 V	
59	ANTCTL0*	DO, PD	Antenna control	1.8 V	
60	WLAN_PA_EN	DI	Self-protection for QLN4650 control	1.8 V	
61	ANTCTL1*	DO, PD	Antenna control	1.8 V	
62	COEX_RXD*	DI, PD	LTE/WLAN coexistence receive	1.8 V	
63	ANTCTL2*	DO, PD	Antenna control	1.8 V	
64	COEX_TXD*	DO, PD	LTE/WLAN coexistence transmit	1.8 V	
65	ANTCTL3*	DO, PD	Antenna control	1.8 V	
66	USIM1_DET	DI, PU	(U)SIM1 card hot-plug detect	1.8 V	Internally pulled up to 1.8 V [1]
67	RESET#	DI, PU	Reset the module. Active LOW.	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V with a 40 kΩ resistor.
68	ANT_CONFIG	DI, PU	Antenna configuration	1.8 V	Internally pulled up to 1.8 V
69	CONFIG_1	DO	Connected to GND internally		
70	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	

71	GND		Ground	
72	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
73	GND		Ground	
74	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
75	CONFIG_2	DO	Not connected internally	

NOTES

1. [1)] This pin is pulled up by software configuration when (U)SIM hot-plug is enabled by **AT+QSIMDET** (the command takes effect after the module is restarted, see ***document [3]***).
2. [2)] RFFE_CLK and RFFE_DATA are reserved only for customization.
3. Keep all NC, reserved and unused pins unconnected.

2.6. Evaluation Board

To help you develop applications conveniently with EM120R-GL and EM160R-GL, Quectel supplies an evaluation board (PCIE-CARD-EVB). For more details, see ***document [2]***.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of EM120R-GL and EM160R-GL.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connected. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command sets the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** command or driving W_DISABLE1# pin low will set the module to airplane mode. In this mode, the RF function is invalid.	
Sleep Mode	The module keeps receiving paging messages, SMS, voice calls and TCP/UDP data from the network with its current consumption reducing to the minimal level.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all interfaces are inaccessible, and the operating voltage (connected to VCC) remains applied.	

3.1.1. Sleep mode

In sleep mode, DRX of the module is able to reduce the current consumption to a minimum level, and DRX cycle index values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current consumption in sleep mode. The longer the DRX cycle is, the lower the current consumption will be.

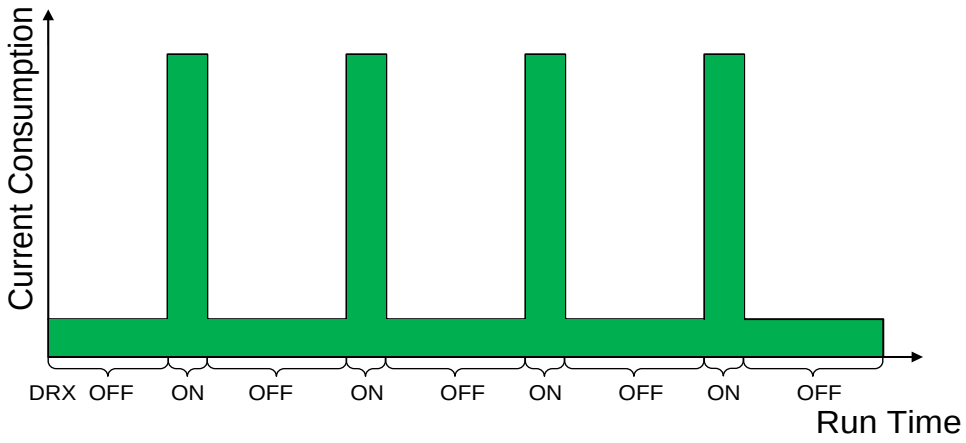


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following part of this section describes the power saving procedure and sleep mode entrance of the module.

If the host supports USB suspend/resume and remote wakeup function, the following two conditions must be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- The host's USB bus, which is connected to the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

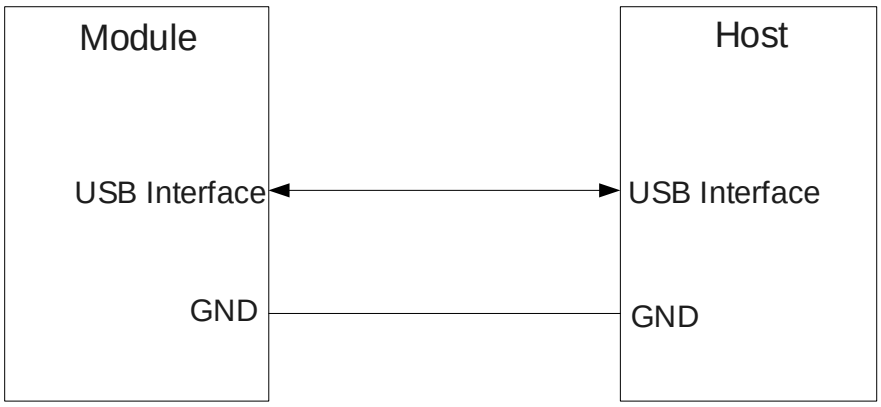


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will wake up in the following conditions:

- Sending data to module through USB will wake up the module.
- When module has a URC to report, the module will send remote wake-up signals via USB bus to wake up the host.

3.1.2. Airplane mode

The module provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. See ***Chapter 4.5.1*** for more details

3.2. Communication Interface with the Host

The module supports to communicate through both USB and PCIe interfaces, respectively referring to the USB mode and the PCIe mode as described below:

USB Mode

- Support all USB 2.0/3.0 features
- Support MBIM/QMI/QRTR/AT

USB is the default communication interface between the module and the host. It is suggested that USB 2.0 interface be reserved for firmware upgrade.

PCIe Mode (eFuse-based)

- Support MBIM/QMI/QRTR/AT
- Support Non-X86 systems and X86 system (support BIOS PCIe early initial)

EM120R-GL and EM160R-GL can also be reprogrammed to PCIe mode based on eFuse. If the communication is switched to PCIe mode by burnt eFuse, the communication cannot be switched back to USB mode.

3.3. Power Supply

The following table shows pin definition of VCC pins and ground pins.

Table 7: Definition of VCC and GND Pins

Pin No.	Pin Name	I/O	Description	DC Characteristics
2, 4, 70, 72, 74	VCC	PI	Power supply	3.135–4.4 V 3.7 V typical DC supply
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND		Ground	

3.3.1. Decrease Voltage Drop

The power supply range of the module is from 3.135 V to 4.4 V. Please ensure that the input voltage will never drop below 3.135 V, otherwise the module will be powered off automatically. The following figure shows the maximum voltage drop during radio transmission in 3G/4G networks.

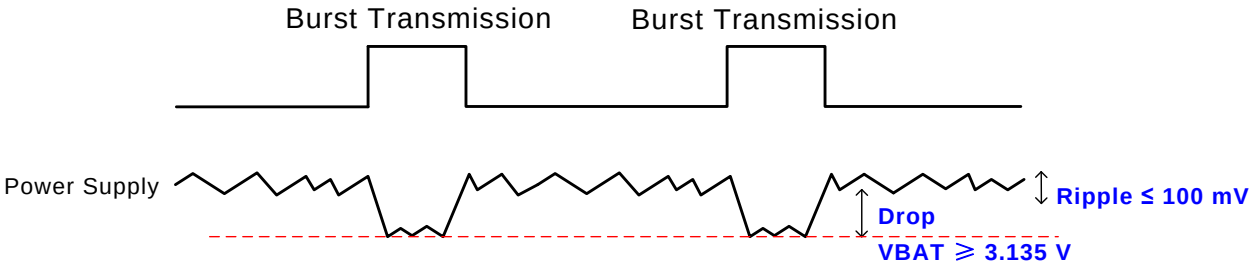


Figure 5: Power Supply Limits during Radio Transmission

Ensure the continuous current capability of the power supply is 2.0 A. To decrease the voltage drop, two bypass capacitor of about 220 μF with low ESR (ESR = 0.7 Ω) should be used. To decrease the power supply is disturbed, a multi-layer ceramic chip capacitor (MLCC) array also should be used due to its ultra-low ESR. It is recommended to use four ceramic capacitors (1 μF, 100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The width of VCC trace should be no less than 2.5 mm. In principle, the longer the VCC trace is, the wider it should be.

In addition, to guarantee stability of the power supply, please use a zener diode with a reverse zener voltage of 5.1 V and a dissipation power of higher than 0.5 W. The following figure shows a reference circuit for the VCC.

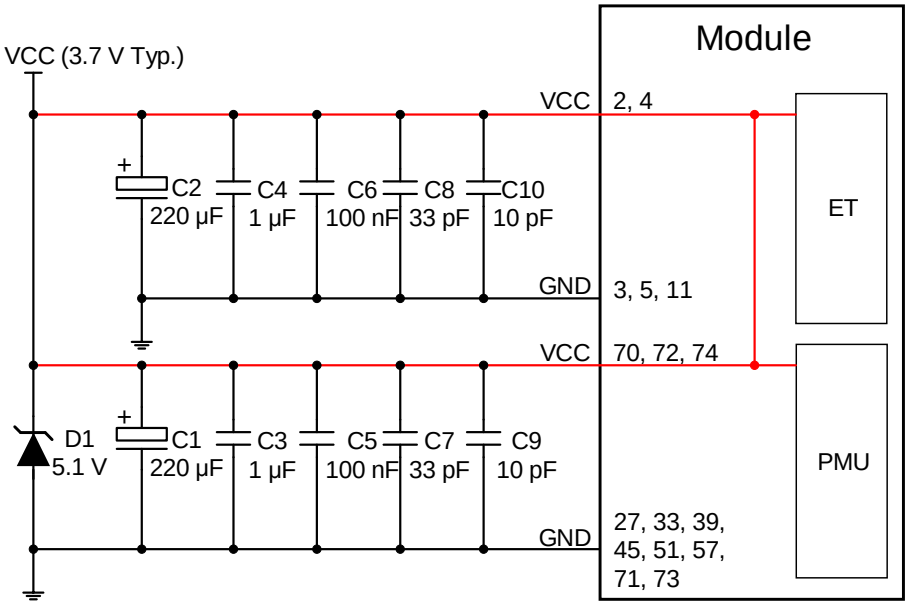


Figure 6: Reference Circuit for the VCC

3.3.2. Reference Design for Power Supply

Power design is important for the module, as the performance of the module largely depends on the power source. If the voltage difference between the input and output is not too high, it is suggested that an LDO is used when supplying power for the module. If there is a big voltage difference between the input source and the desired output (VCC = 3.7 V Typ.), a buck DC-DC converter is preferred.

The following figure shows a reference design for +5 V input power source based on the DC-DC TPS54319. The typical output of the power supply is about 3.7 V and the maximum load current is 3.0 A.

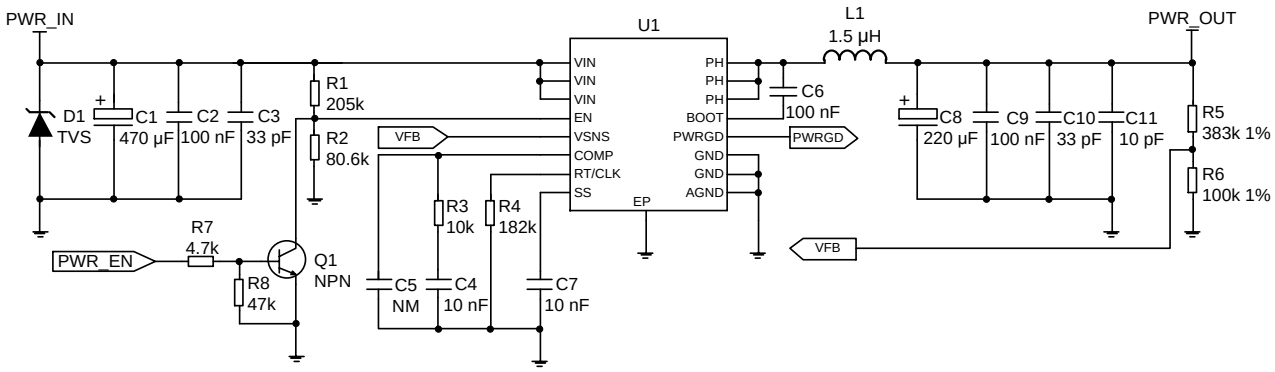


Figure 7: Reference Circuit for the Power Supply

NOTE

To avoid damaging the internal flash, do not switch off the power supply directly when the module is working.

3.4. Turn on

FULL_CARD_POWER_OFF# is used to turn on/off the module. When the input signal is asserted high (≥ 1.19 V), the module will be turned on. When the input signal is driven low (≤ 0.2 V) or Tri-stated, the module will be turned off.

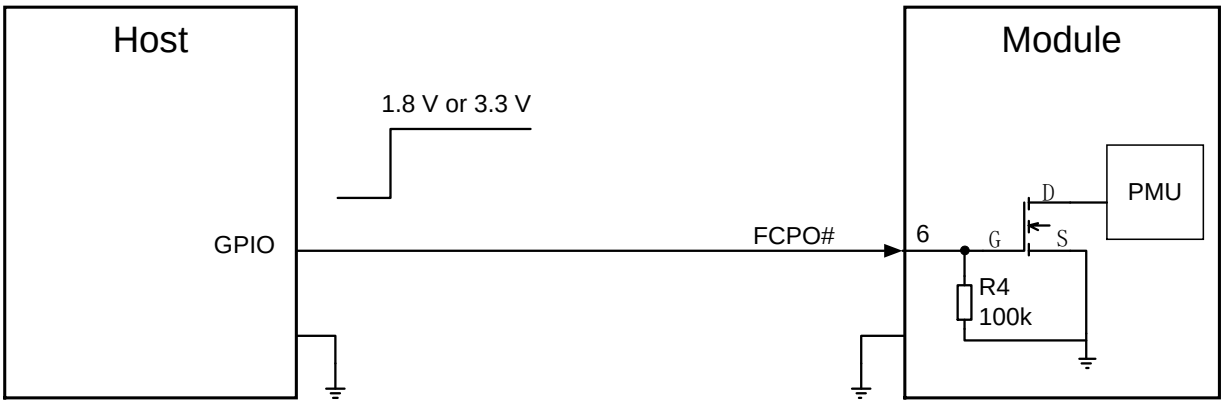
This input signal is 3.3 V tolerant and can be driven by either 1.8 V or 3.3 V GPIO. Also, it has internally pulled down with a 100 kΩ resistor.

The following table shows the definition of FULL_CARD_POWER_OFF#.

Table 8: Pin Definition of FULL_CARD_POWER_OFF#

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
6	FULL_CARD_ POWER_OFF#	DI, PD	Turn on/off the module. High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Pull down with a 100 kΩ resistor.

It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated in the following figure.



Note: The voltage of pin 6 should be no less than 1.19 V when it is at HIGH level.

Figure 8: Turn on the Module with a Host GPIO

The timing of turn-on scenario is illustrated in the following figure.

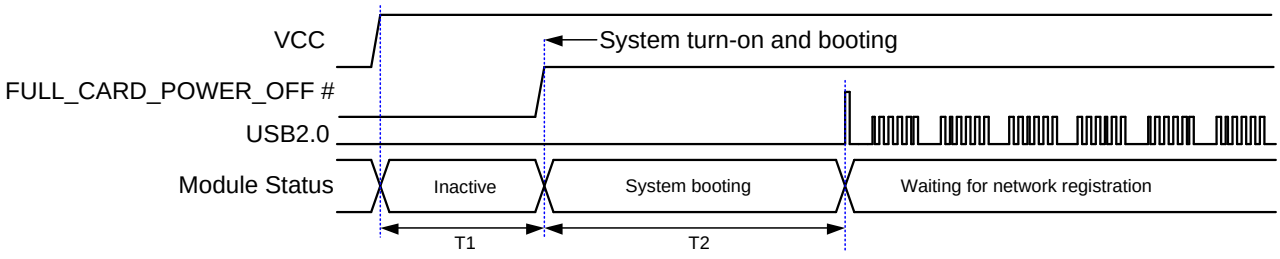


Figure 9: Turn-on Timing of the Module

Table 9: Turn-on Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T1	0 ms	50 ms	-	Module power on
T2	9.3 s	-	-	

3.5. Turn off

For the design that turns on the module with a host GPIO, when the power is supplied to VCC, pulling down FULL_CARD_POWER_OFF# pin will turn off the module.

The timing of turn-off scenario is illustrated in the following figure.

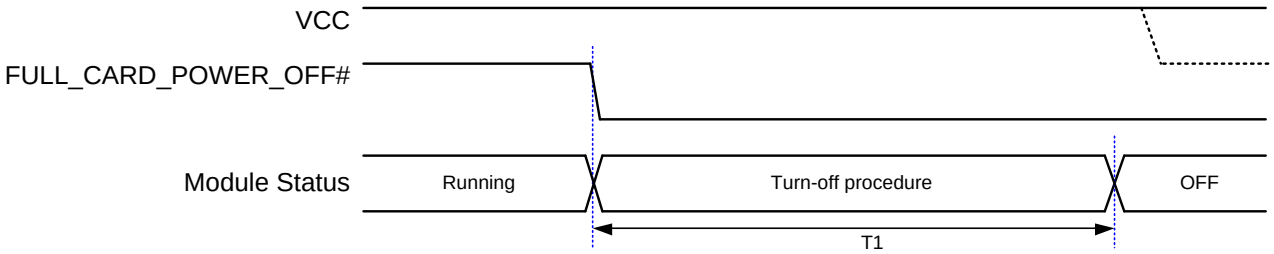


Figure 10: Turn-off Timing through FULL_CARD_POWER_OFF#

Table 10: Turn-off Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T1	3 s		-	Module turns off

3.6. Reset

The RESET# pin is used to reset the module. The module can be reset by driving RESET# low voltage for 250–600 ms.

Table 11: Pin Definition of RESET#

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
67	RESET#	DI, PU	Reset the module Active LOW.	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V with a 40 kΩ resistor.

NOTE

Triggering the RESET# signal will lead to loss of all data in the modem and removal of system drivers. It will also disconnect the modem from the network.

The module can be reset by pulling down the RESET# pin for 250–600 ms. An open collector/drain driver or a button can be used to control the RESET# pin.

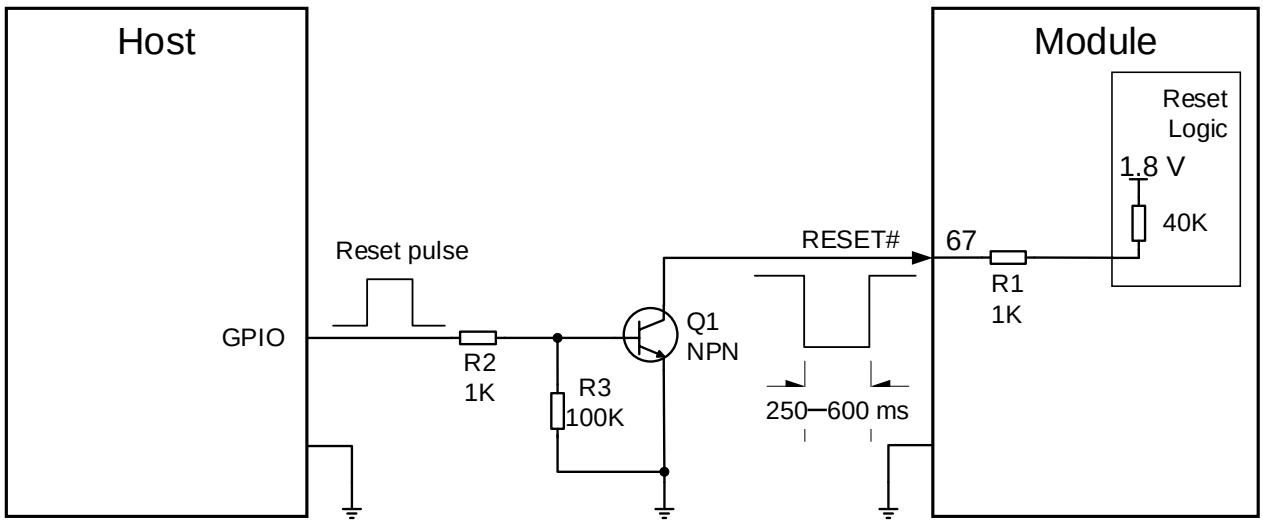
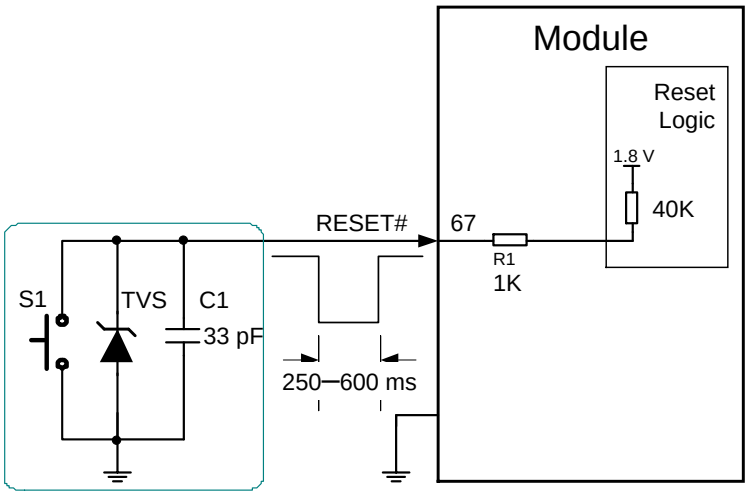


Figure 11: Reference Circuit for the RESET# with NPN Driver Circuit



Note: The capacitor C1 is recommended to be less than 47 pF.

Figure 12: Reference Circuit for the RESET# with A Button

The timing of reset scenario is illustrated in the following figure.

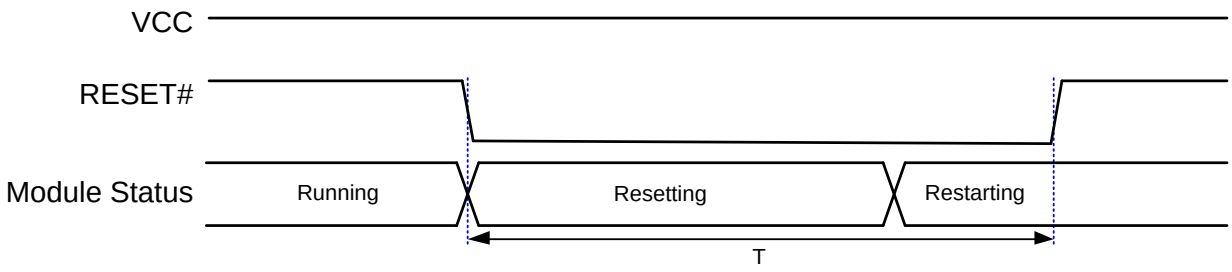


Figure 13: Reset Timing of the Module

Table 12: Reset Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T	250 ms	500 ms	600 ms	RESET# should be pulled down for 250–600 ms. An asserting time of less than 200 ms is unreliable, while that of higher than 600 ms may lead to module reset for several times.

4 Application Interfaces

The physical connections and signal levels of EM120R-GL and EM160R-GL comply with *PCI Express M.2 specification*. This chapter mainly describes the definition and application of the following interfaces/pins of the module:

- (U)SIM interfaces
- USB interface
- PCIe interface
- PCM interface*
- Control and indication interfaces
- Cellular/WLAN COEX interface*
- Antenna tuner control interface*
- Configuration pins

4.1. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported, and Dual SIM Single Standby function is supported.

4.1.1. Pin definition of (U)SIM

The module has two (U)SIM interfaces.

Table 13: Pin Definition of (U)SIM Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics
36	USIM1_VDD	PO	Power supply for (U)SIM1 card	1.8/3.0 V
34	USIM1_DATA	DIO, PU	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V
32	USIM1_CLK	DO, PD	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V
30	USIM1_RST	DO, PD	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V

66	USIM1_DET	DI, PU	(U)SIM1 card hot-plug detection	1.8 V
40	USIM2_DET*	DI, PU	(U)SIM2 card hot-plug detection	1.8 V
42	USIM2_DATA	DIO, PU	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V
44	USIM2_CLK	DO, PD	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V
46	USIM2_RST	DO, PD	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V
48	USIM2_VDD	PO	Power supply for (U)SIM2 card	1.8/3.0 V

NOTES

USIM_DET[1:2] is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.2. (U)SIM Hot-plug

The module supports (U)SIM card hot-plug via (U)SIM card hot-plug detection pins (USIM_DET[1:2]). (U)SIM card insertion is detected by high/low level. (U)SIM card hot-plug is disabled by default.

The following command enables (U)SIM card hot-plug function.

AT+QSIMDET (U)SIM Card Detection	
Test Command **AT+QSIMDET=?**	Response **+QSIMDET: (**list of supported **<enable>**s**),(**list of supported **<insert_level>**s**)** **OK**
Read Command **AT+QSIMDET?**	Response **+QSIMDET: <enable>,<insert_level>** **OK**
Write Command **AT+QSIMDET=<enable>,<insert_level>**	Response **OK** If there is any error: **ERROR**
Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved to NVRAM automatically.

Parameter

<enable>	Integer type. Enable or disable (U)SIM card detection. 0 Disable 1 Enable
<insert_level>	Integer type. The level of (U)SIM detection pin when a (U)SIM card is inserted. 0 Low level 1 High level

NOTES

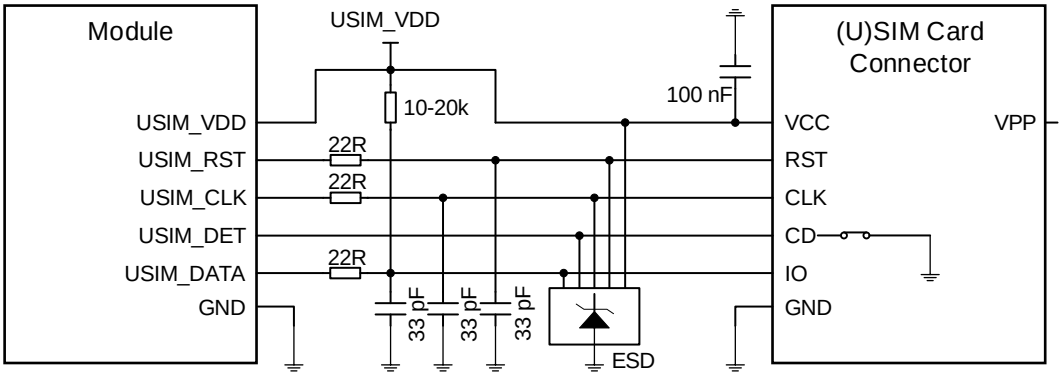
1. Hot-plug function is invalid if the configured value of **<insert_level>** is inconsistent with hardware design.
2. The underlined value is the default parameter value.
3. USIM_DET[1:2] is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.3. Normally Closed (U)SIM Card Connector

With a normally closed (U)SIM card connector, USIM_DET pin is normally shorted to ground when there is no (U)SIM card inserted. (U)SIM card detection by high level is applicable to this type of connector. After executing **AT+QSIMDET=1,1** to enable the (U)SIM hot-plug: when a (U)SIM card is inserted, USIM_DET will change from low to high level; when the (U)SIM card is removed, USIM_DET will change from high to low level.

- When the (U)SIM is absent, CD is shorted to ground and USIM_DET is at low level.
- When the (U)SIM is present, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design of (U)SIM interface with a normally closed (U)SIM card connector.



Note: All these resistors, capacitors and ESD should be close to (U)SIM card connector in PCB layout.

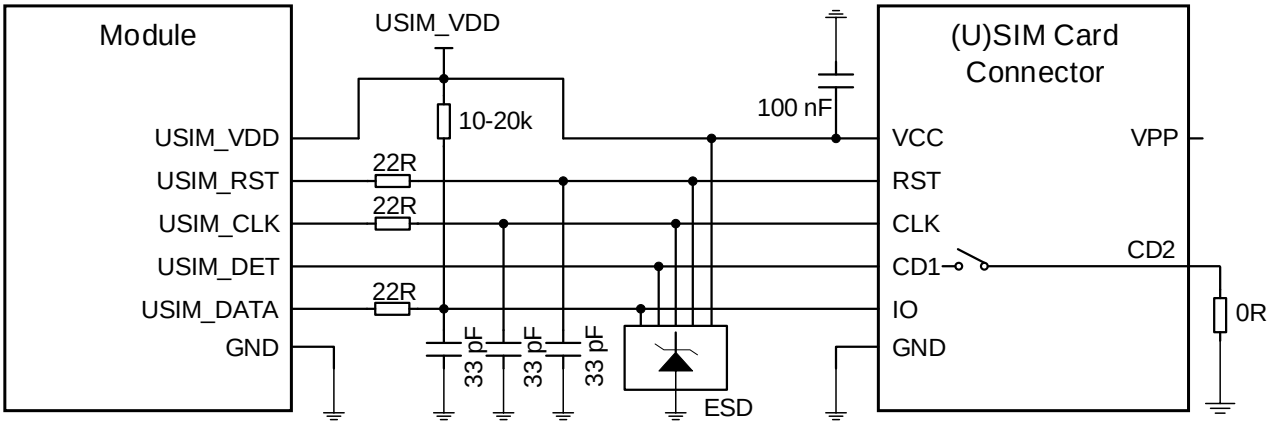
Figure 14: Reference Circuit for Normally Closed (U)SIM Card Connector

4.1.4. Normally Open (U)SIM Card Connector

With a normally open (U)SIM card connector, CD1 and CD2 of the connector are disconnected when there is no (U)SIM card inserted. (U)SIM card detection by low level is applicable to this type of connector. After executing **AT+QSIMDET=1,0** to enable the (U)SIM hot-plug: when a (U)SIM card is inserted, USIM_DET will change from high to low level; when the (U)SIM card is removed, USIM_DET will change from low to high level.

- When the (U)SIM is absent, CD1 is open from CD2 and USIM_DET is at high voltage level.
- When the (U)SIM is inserted, CD1 is short-circuited to CD2 and USIM_DET is at low voltage level.

The following figure shows a reference design of (U)SIM interface with a normally open (U)SIM card connector.

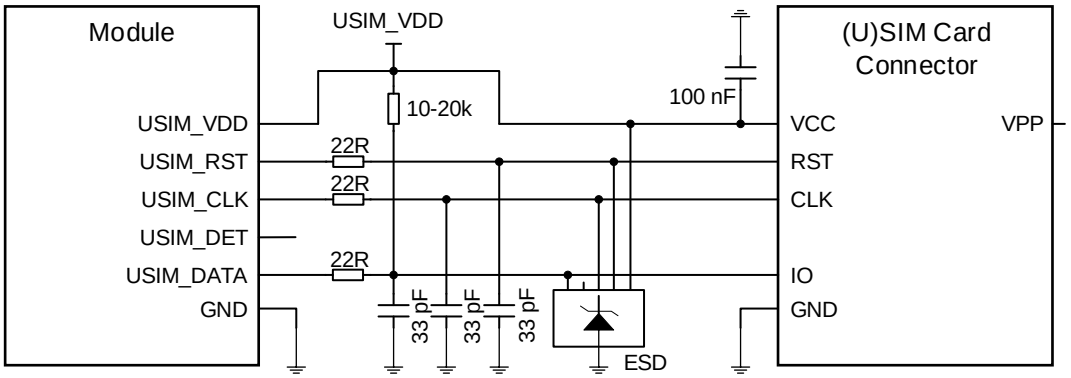


NOTE:
All these resistors, capacitors and ESD should be close to (U)SIM card connector in PCB layout.

Figure 15: Reference Circuit for Normally Open (U)SIM Card Connector

4.1.5. (U)SIM Card Connector Without Hot-plug

If the (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for the (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated by the following figure.



Note: All these resistors, capacitors and ESD should be close to (U)SIM card connector in PCB layout.

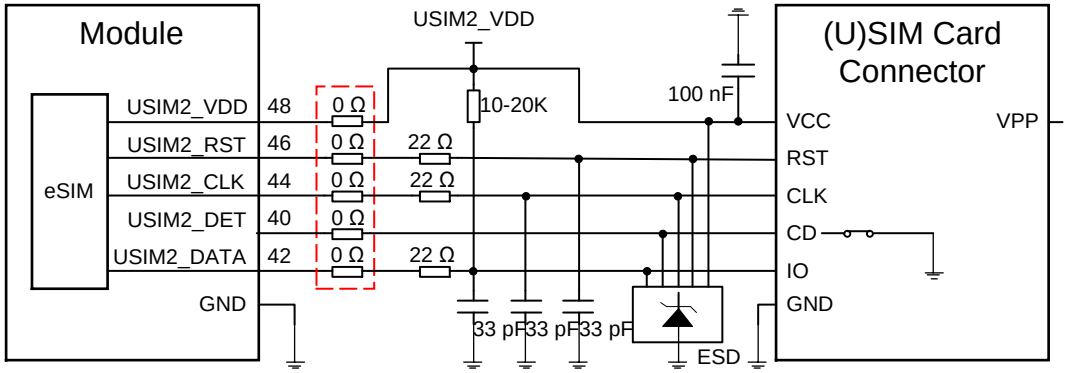
Figure 16: Reference Circuit for a 6-Pin (U)SIM Card Connector

4.1.6. (U)SIM2 Card Connector

EM120R-GL and EM160R-GL provide two (U)SIM interfaces. (U)SIM1 interface is used for external (U)SIM card only, and (U)SIM2 interface is used for external (U)SIM card or internal eSIM card.

It should be noted that when the (U)SIM2 interface is used for an external (U)SIM card, the circuits are the same as those of (U)SIM1 interface. When the (U)SIM2 interface is used for the internal eSIM card, pins 40, 42, 44, 46 and 48 of the module must be kept open.

A recommended compatible design for the (U)SIM2 interface is shown below.



Note: The five 0 Ω resistors must be close to M.2 socket connector, and all other components should be close to (U)SIM card connector in PCB layout.

Figure 17: Recommended Compatible Design for (U)SIM2 Interface

4.1.7. (U)SIM Design Notices

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm.
- Keep (U)SIM card signals away from RF and VCC traces.
- Make sure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS diode array of which the parasitic capacitance should be not higher than 10 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to suppress EMI such as spurious transmission. The 33 pF capacitors are used to filter out RF interference. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- For USIM_DATA, a 10–20 kΩ pull-up resistor must be added near the (U)SIM card connector.

4.2. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0 & 2.0 specifications and supports super speed (5 Gbps) on USB 3.0 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB*.

Please note that only USB 2.0 can be used for firmware upgrade currently.

Table 14: Pin Definition of USB Interface

Pin No.	Pin Name	I/O	Description	Comment
7	USB_DP	AIO	USB differential data bus (+)	Require differential impedance of 90 Ω
9	USB_DM	AIO	USB differential data bus (-)	
29	USB_SS_TX_M	AO	USB 3.0 super-speed transmit (-)	
31	USB_SS_TX_P	AO	USB 3.0 super-speed transmit (+)	
35	USB_SS_RX_M	AI	USB 3.0 super-speed receive (-)	

37	USB_SS_RX_P	AI	USB 3.0 super-speed receive (+)

For more details about the USB 3.0 & 2.0 specifications, please visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in designs. The following figure presents a reference circuit for the USB 3.0 & 2.0 interface.

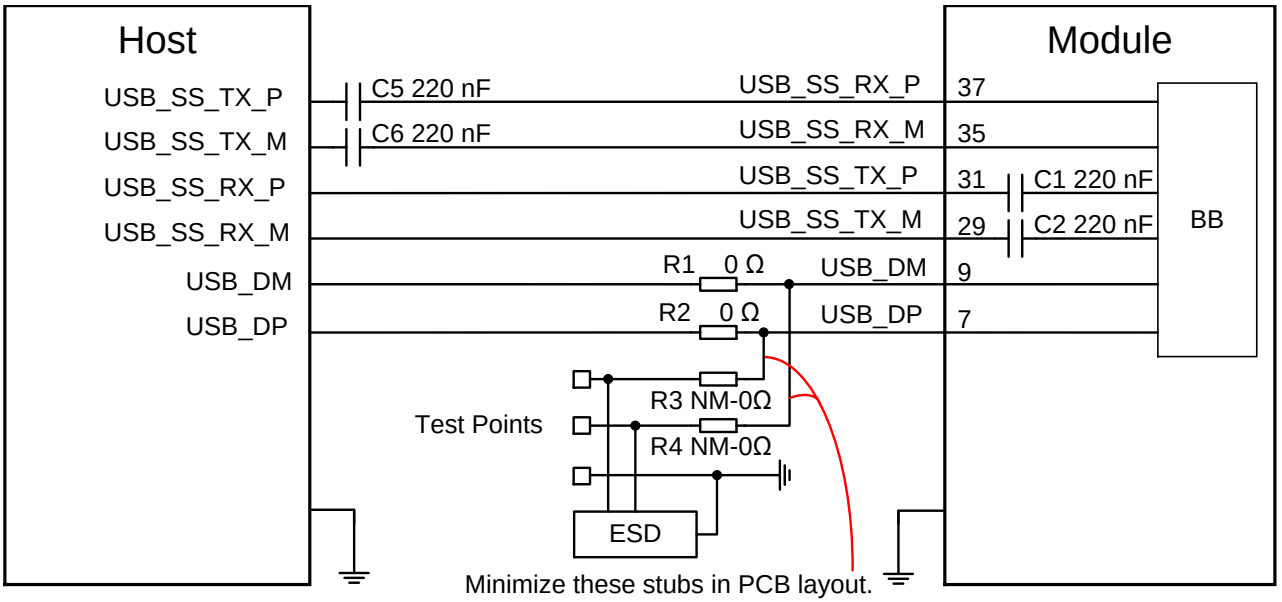


Figure 18: Reference Circuit for the USB 3.0 & 2.0 Interface

AC coupling capacitors C5 and C6 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB. To ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 must be placed close to the module, and the stubs must be minimized in PCB layout.

Please follow the principles below when designing for the USB interface to meet USB 3.0 and 2.0 specifications:

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of differential trace of USB 2.0 and USB 3.0 is 90 Ω.
- For USB 2.0 signal traces, the trace length should be less than 120 mm, and the differential data pair matching should be less than 2 mm. For USB 3.0 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.7 mm, while the matching between Tx and Rx should be less than 10 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data lines, so you

should pay attention to the selection of the device. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.0.

- Keep the ESD protection devices as close to the USB connector as possible.
- If possible, reserve 0 Ω resistors on USB_DP and USB_DM lines respectively.

4.3. PCIe Interface

The module provides one integrated PCIe interface, featuring as follows:

- *PCI Express Base Specification Revision 2.0* compliant
- Data rate up to 5 Gbps per lane

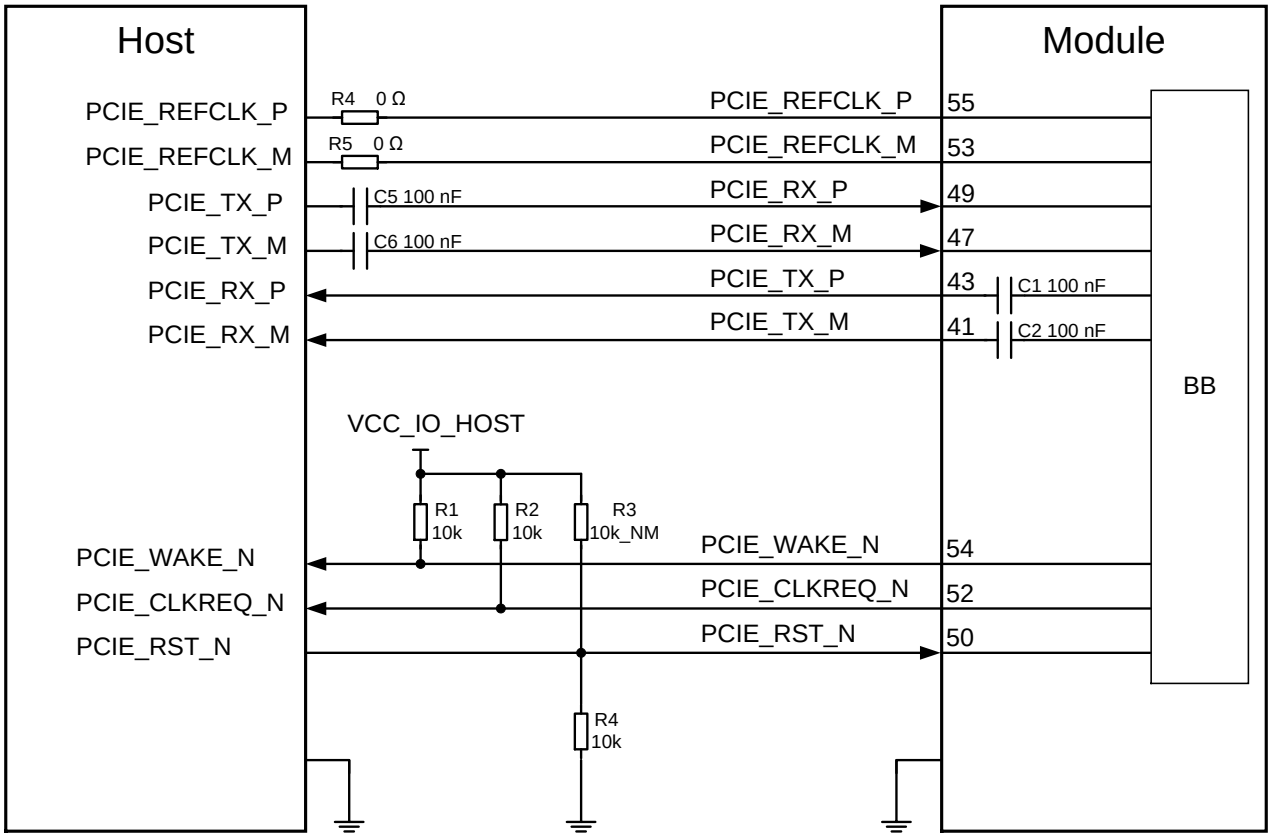
4.3.1. Pin definition of PCIe

Table 15: Pin Definition of PCIe Interface

Pin No.	Pin Name	I/O	Description	Comment
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	100 MHz clock frequency. Require differential impedance of 95 Ω
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	
49	PCIE_RX_P	AI	PCIe receive (+)	Require differential impedance of 95 Ω
47	PCIE_RX_M	AI	PCIe receive (-)	
43	PCIE_TX_P	AO	PCIe transmit (+)	Require differential impedance of 95 Ω
41	PCIE_TX_M	AO	PCIe transmit (-)	
50	PCIE_RST_N	DI, OD	PCIe reset. Active LOW.	
52	PCIE_CLKREQ_N	DO, OD	PCIe clock request. Active LOW.	
54	PCIE_WAKE_N	DO, OD	PCIe wake up. Active LOW.	

4.3.2. Reference Design for PCIe

The following figure shows a reference circuit for the PCIe interface.



Note. The voltage level VCC_IO_HOST of these three signals depend on the host side due to open drain.

Figure 19: PCIe Interface Reference Circuit

To ensure the signal integrity of PCIe interface, AC coupling capacitors C5 and C6 should be placed close to the host on PCB. C1 and C2 have been integrated into the module, so do not place these two capacitors on your schematic and PCB.
The following principles of PCIe interface design should be complied with, to meet the PCIe specification.

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, crystal and oscillator signals.
- Add a capacitor in series on Tx/Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx) less than 0.7 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as 95 Ω ±10 %.
- You must not route PCIe data traces under components or cross them with other traces.

4.3.3. PCIe Timing

The following figure is PCIe power-on timing sequence for an adapter powered from system power rail in PCI Express M.2 specification.

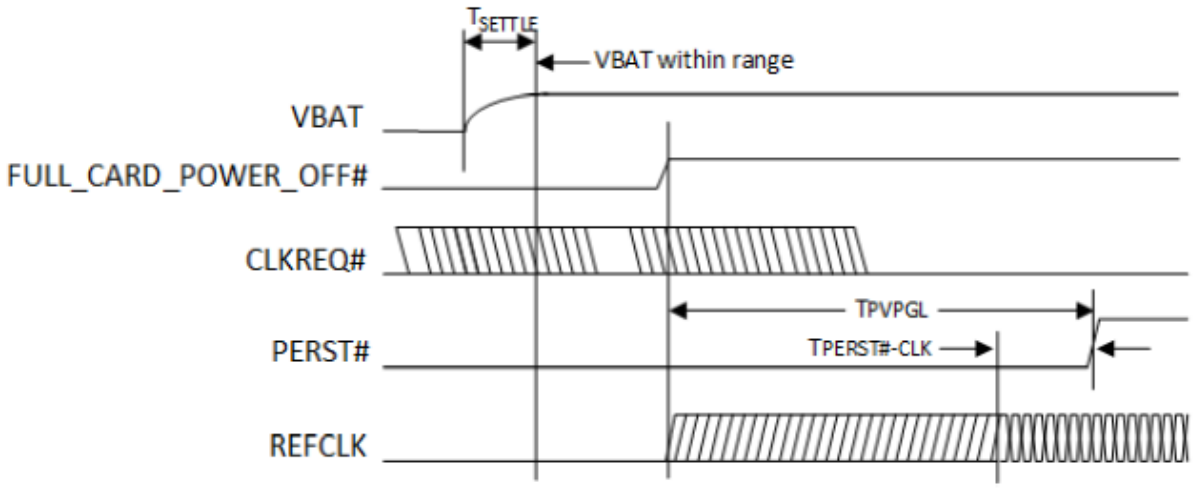


Figure 20: PCIe Power-on Timing Requirements of M.2 Specification

The following table is power-on timing variables in PCI Express M.2 specification.

Table 16: Power-up Timing of M.2 Specification

Symbol	Min.	Typ.	Max.	Comment
T_{PVPGL}	50 ms	-	-	Power valid to PERST# input inactive
$T_{PERST\#-CLK}$	100 µs	-	-	REFCLK stable before PERST# inactive

4.3.3.1. PCIe Turn-on Timing

If FULL_CARD_POWER_OFF# is de-asserted, the module will turn on. RESET# is pulled up inside the module. Keep RESET# floating or at high level during module power-on.

PCIe turn-on timing is illustrated by the following figure.

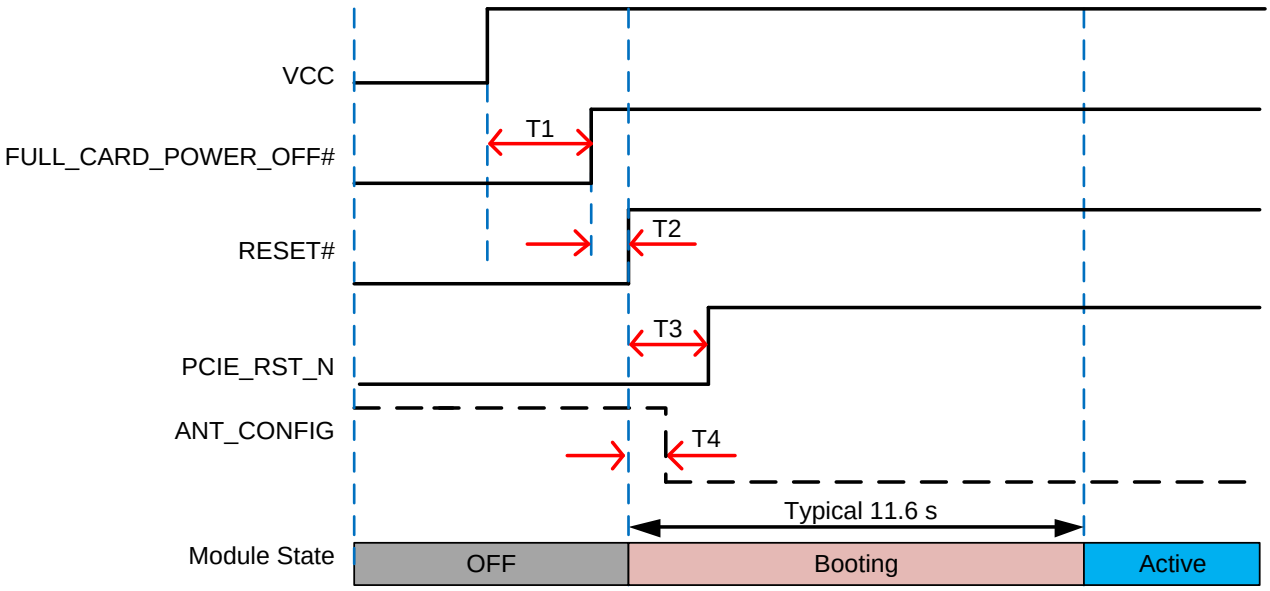


Figure 21: PCIe Turn-on Timing of the Module

Table 17: PCIe Turn-on Timing of the Module

Index	Min.	Typ.	Max.	Comment
T1	0 ms	50 ms	-	The module is turning on.
T2	0 ms	-	200 ms	De-assert RESET# after de-asserting FULL_CARD_POWER_OFF#.
T3	100 ms	-	-	De-assert PCIE_RST_N 100 ms after de-asserting RESET#.
T4	0 ms	-	T3	● ANT_CONFIG is used for the antenna configuration of EM160R-GL module. High/Floating: 2 antennas (high by default); Low: 4 antennas. ● If ANT_CONFIG is not used, T4 could be ignored. Assert ANT_CONFIG before de-asserting PCIE_RST_N.

4.3.3.2. PCIe Turn−off Timing

The module will turn off after FULL_CARD_POWER_OFF# is asserted. This is a way to turn off the module via software.

PCIe turn-off timing is illustrated by the following figure.

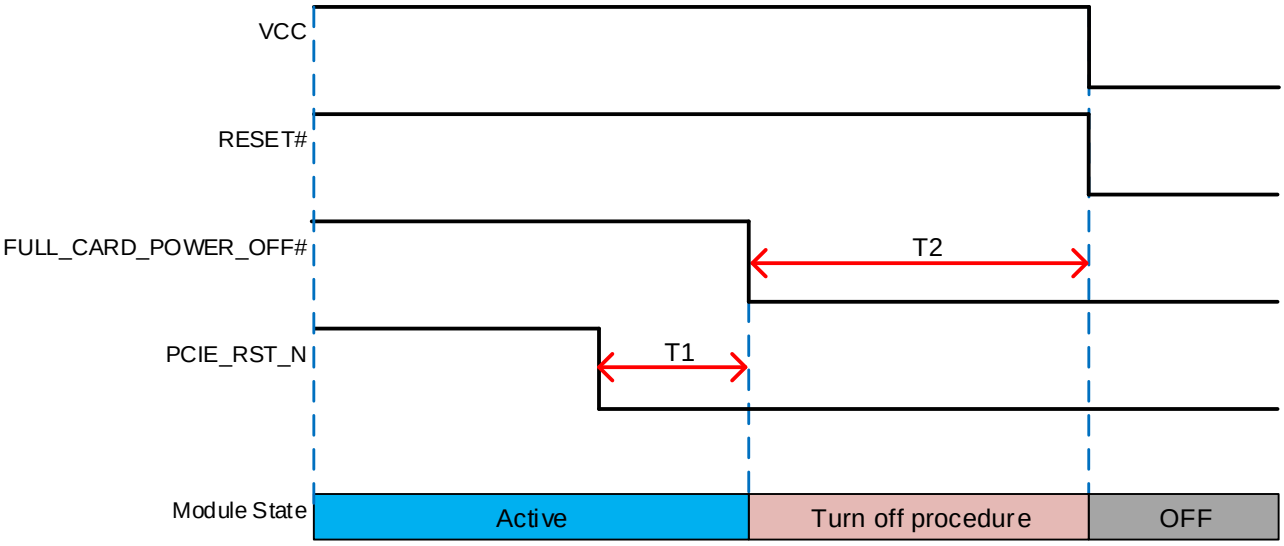


Figure 22: PCIe Turn-off Timing through FULL_CARD_POWER_OFF#

Table 18: PCIe Turn-off Timing through FULL_CARD_POWER_OFF#

Index	Min.	Typ.	Max.	Comment
T1	20 ms	-	-	PCIe interface is disabled by asserting PCIE_RST_N.
T2	3 s	-	-	Module is turning off and it stops reading and writing Flash, data protection, etc. If the power is always on, T2 could be ignored.

4.3.3.3. PCIe Reset Timing

RESET# pin is used to reset the module. FULL_CARD_POWER_OFF# is driven LOW during system reset.

PCIe reset timing is illustrated by the following figure.

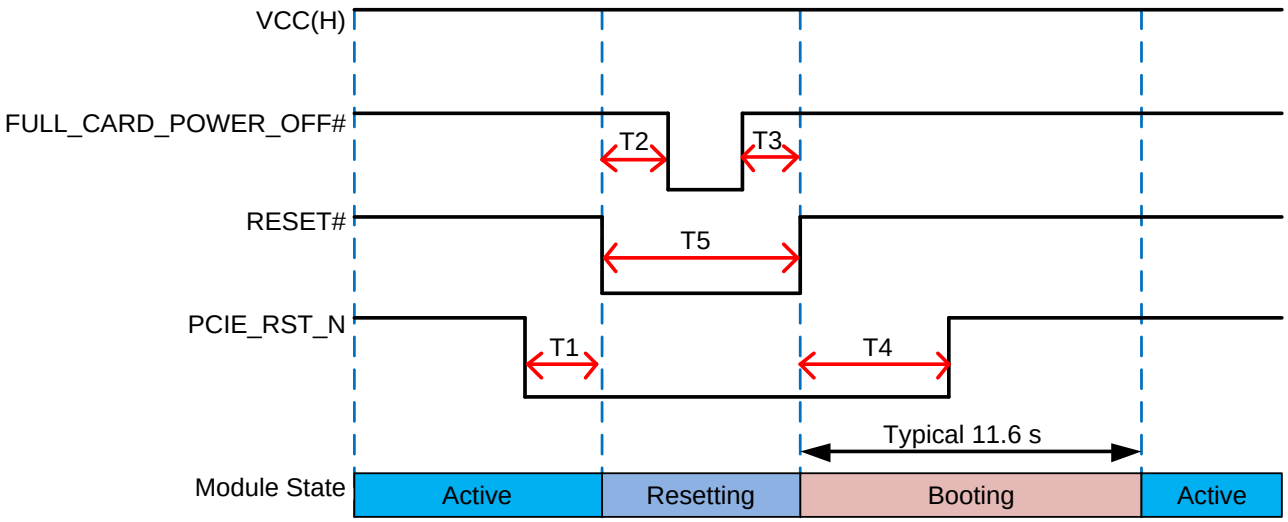


Figure 23: PCIe Reset Timing

Table 19: PCIe Reset Timing

Index	Min.	Typ.	Max.	Comment
T1	20 ms	-	-	PCIe interface is disabled by asserting PCIE_RST_N.
T2	0 ms	-	-	Module is reset by asserting RESET#.
T3	0 ms	-	-	T3 could be ignored.
T4	100 ms	-	-	De-assert PCIE_RST_N 100 ms after de-asserting RESET#.
T5	250 ms	500 ms	-	

4.3.3.4. PCIe Modern Standby Timing

EM120R-GL and EM160R-GL support D3 Hot and D3 Cold state in Win10 system. When the module enters D3 Hot or D3 Cold state, the timing is shown below:

- **D3 Hot Timing**

In D3 Hot state, PCIE_RST_N remains at high level.

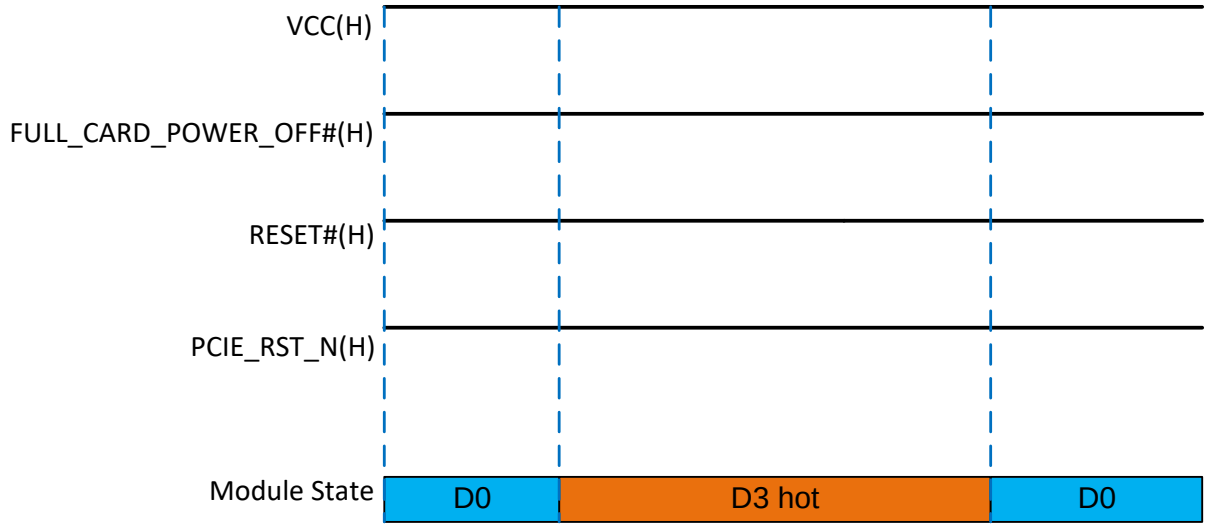


Figure 24: PCIe D3 Hot State Timing

- **D3 Cold Timing**

The module must go through D3 Hot before entering D3 Cold state. In D3 Hot state, PCIE_RST_N remains at high level, then in D3 cold state, PCIE_RST_N should be pulled down.

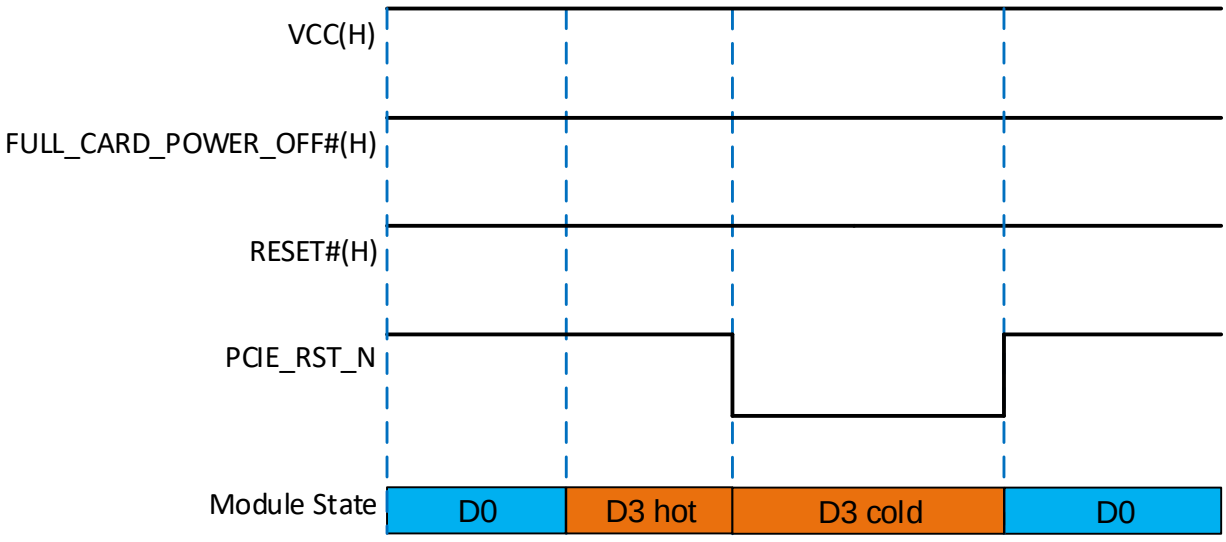


Figure 25: PCIe D3 Cold Timing

4.4. PCM Interface*

The module supports audio communication via Pulse Code Modulation (PCM) digital interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave
- Auxiliary mode (long frame synchronization): the module works as master only

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

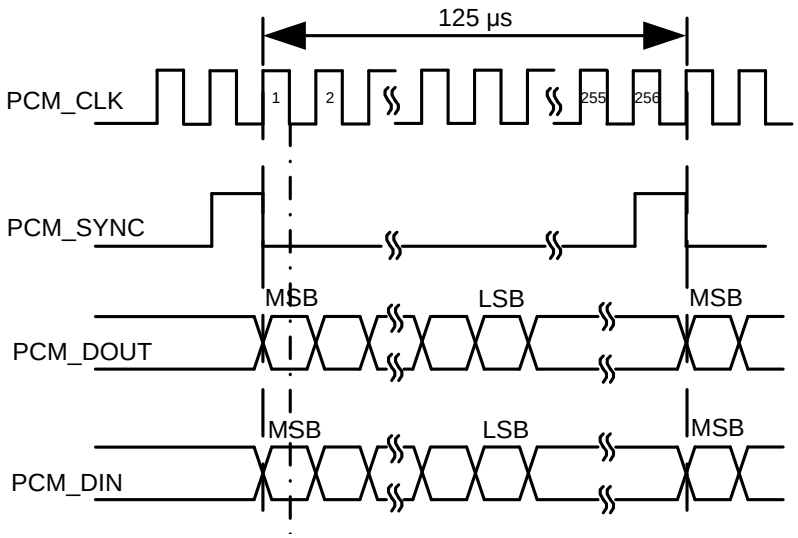


Figure 26: Primary Mode Timing

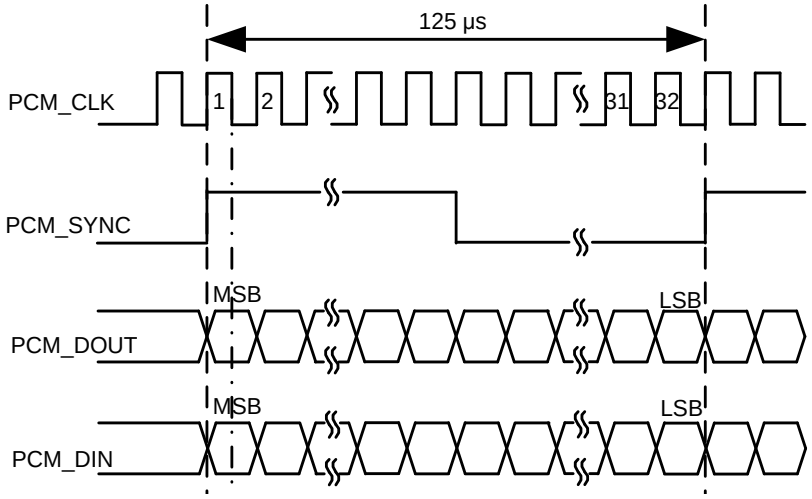


Figure 27: Auxiliary Mode Timing

The following table shows the pin definition of PCM interface which can be applied to audio codec design.

Table 20: Pin Definition of PCM Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
20	PCM_CLK*	DIO, PD	PCM clock	1.8 V
22	PCM_DIN*	DI, PD	PCM data input	1.8 V
24	PCM_DOUT*	DO, PD	PCM data output	1.8 V
28	PCM_SYNC*	DIO, PD	PCM data frame sync	1.8 V

The clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [3]*** for details about **AT+QDAI** command.

4.5. Control and Indication Interfaces

Table 21: Pin Definition of Control and Indication Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics
8	W_DISABLE1#	DI, OD	Airplane mode control. Active LOW.	1.8/3.3 V

10	WWAN_LED#	DO, OD	RF status indication LED. Active LOW.	VCC
23	WAKE_ON_WAN#*	DO, OD	Wake up the host. Active LOW.	1.8/3.3 V
25	DPR	DI, PU	Dynamic power reduction. High voltage level by default.	1.8 V
26	W_DISABLE2#	DI, OD	GNSS disable control. Active LOW.	1.8/3.3 V
60	WLAN_PA_EN	DI, PD	Self-protection of QLN4650 control	1.8 V
68	ANT_CONFIG	DI, PU	Antenna configuration	1.8 V

4.5.1. W_DISABLE1#

The module provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. W_DISABLE1# is pulled up by default. Driving it low will set the module to airplane mode. In airplane mode, the RF function will be disabled.

The RF function can also be enabled or disabled through software AT commands. The following table shows the RF function status of the module.

Table 22: RF Function Status

W_DISABLE1# Level	AT Commands	RF Function Status
High Level	**AT+CFUN=1**	Enabled
High Level	**AT+CFUN=0** **AT+CFUN=4**	Disabled
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled

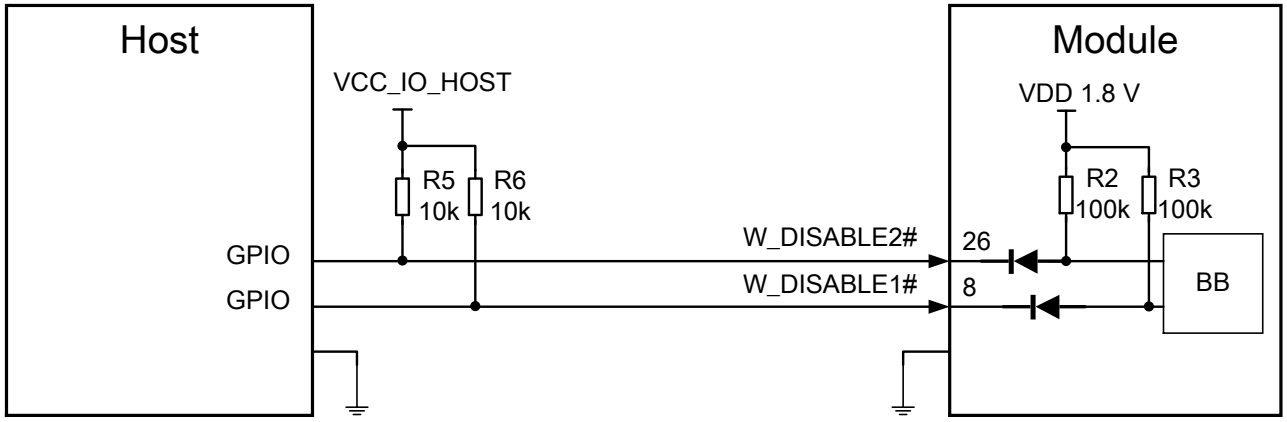
4.5.2. W_DISABLE2#

The module provides a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it low will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands can control the GNSS function.

Table 23: GNSS Function Status

W_DISABLE2# Level	AT Commands	GNSS Function Status
High Level	**AT+QGPS=1**	Enabled
High Level	**AT+QGPSEND**	Disabled
Low Level	**AT+QGPS=1**	
Low Level	**AT+QGPSEND**	

A simple level shifter based on diodes is used on W_DISABLE1# pin and W_DISABLE2# pin which are pulled up to a 1.8 V voltage in the module, as shown in the following figure. So, the control signals (GPIO) of the host device could be at 1.8 V or 3.3 V voltage level. W_DISABLE1# and W_DISABLE2# are active low signals, and a reference circuit is shown as below.



Note: The voltage level of VCC_IO_HOST could be 1.8 V or 3.3 V typically.

Figure 28: W_DISABLE1# and W_DISABLE2# Reference Circuit

4.5.3. WWAN_LED#

The WWAN_LED# signal is used to indicate RF status of the module, and its sink current is up to 10 mA.

To reduce current consumption of the LED, a current-limited resistor must be placed in series with the LED, as illustrated in the figure below. The LED is ON when the WWAN_LED# signal is at low level.

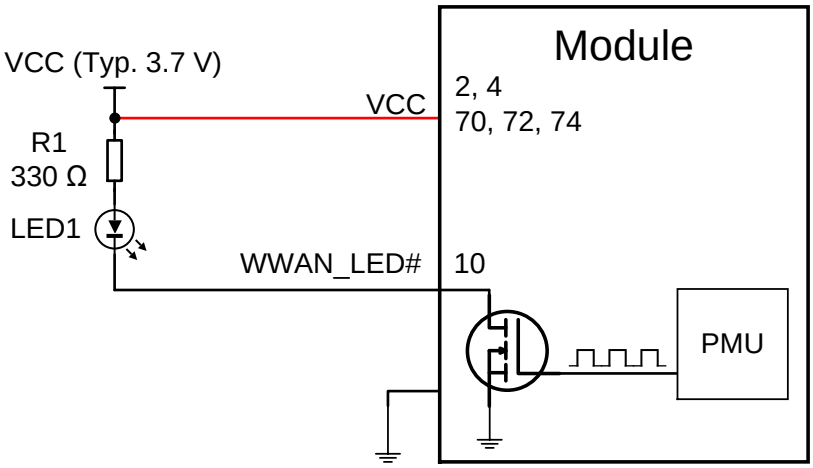


Figure 29: WWAN_LED# Reference Circuit

The following table shows the RF status indicated by WWAN_LED#.

Table 24: Network Status Indications of WWAN_LED#

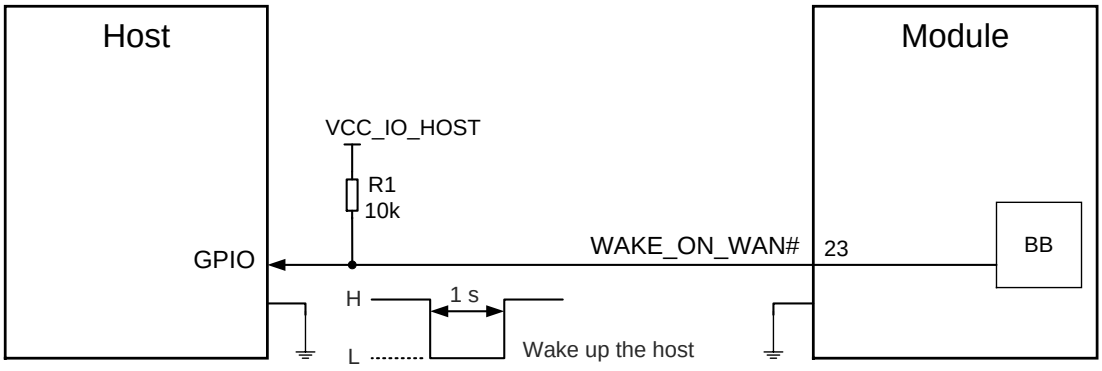
WWAN_LED# Level	Description
Low Level (LED On)	RF function is turned on
High Level (LED Off)	RF function is turned off if any of the following occurs: ● The (U)SIM card is not powered. ● W_DISABLE1# is at low level (airplane mode enabled). ● **AT+CFUN=4** (RF function disabled).

4.5.4. WAKE_ON_WAN#*

The WAKE_ON_WAN# is an open drain pin, which requires a pull-up resistor on the host. When a URC returns, a 1 s low level pulse signal will be outputted to wake up the host. The module operation status indicated by WAKE_ON_WAN# is shown below.

Table 25: State of the WAKE_ON_WAN#

WAKE_ON_WAN# State	Module Operation Status
Output a 1 s low level pulse signal	Call/SMS/Data is incoming (to wake up the host)
Always at high level	Idle/Sleep



Note: The voltage level on VCC_IO_HOST depends on the host side due to the open drain in pin 23.

Figure 30: WAKE_ON_WAN# Signal Reference Circuit

4.5.5. DPR

The module provides the DPR pin for body SAR detection. The signal is sent from a host system proximity sensor to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 26: Function of the DPR Signal

DPR Level	Function
High/Floating	Max transmitting power will NOT backoff.
Low	Max transmitting power backoff by SAR efs file configure.

4.5.6. ANT_CONFIG

EM160R-GL provides an ANT_CONFIG signal for antenna configuration (while EM120R-GL does not support ANT_CONFIG since it only supports 2 antennas). The signal is sent by a host system to EM160R-GL module. ANT_CONFIG is an input port which is pulled high internally by default. The definition of ANT_CONFIG signal is shown as below table.

Table 27: Pin Definition of ANT_CONFIG of EM160R-GL

ANT_CONFIG Level	Function
High/Floating	Support 2 antennas
Low Level	Support 4 antennas

4.5.7. WLAN_PA_EN

QLN4650 enables self-protection circuit (integrated inside QLN4650) when WLAN_PA_EN is ON.

- In LTE mode, the default WLAN_PA_EN is set to 0.
- When WLAN_PA_EN = 1, the LNA will be in self-protection mode.

Table 28: Pin definition of WLAN_PA_EN for EM120R-GL&EM160R-GL

Pin No.	Pin Name	I/O	Description	Comment
60	WLAN_PA_EN	DI, PD	Self-protection of QLN4650 control	1.8 V power domain

4.6. Cellular/WLAN COEX Interface*

The module provides the cellular/WLAN COEX interface, the following table shows the pin definition of this interface.

Table 29: Pin Definition of COEX Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
62	COEX_RXD*	DI, PD	LTE/WLAN coexistence receive	1.8 V
64	COEX_TXD*	DO, PD	LTE/WLAN coexistence transmit	1.8 V

4.7. Antenna Tuner Control Interface*

ANTCTL [0:3] and RFFE interface are used for antenna tuner control and should be routed to an appropriate antenna control circuit. More details about the interface will be added in the future version of this document.

4.7.1. Antenna Tuner Control Interface through GPIOs

Table 30: Pin Definition of Antenna Tuner Control Interface through GPIOs

Pin No.	Pin Name	I/O	Description	DC Characteristics
59	ANTCTL0*	DO, PD	Antenna GPIO Control	1.8 V
61	ANTCTL1*	DO, PD		1.8 V
63	ANTCTL2*	DO, PD		1.8 V
65	ANTCTL3*	DO, PD		1.8 V

4.7.2. Antenna Tuner Control Interface through RFFE

Table 31: Pin Definition of Antenna Tuner Control Interface through RFFE

Pin No.	Pin Name	I/O	Description	DC Characteristics
56	RFFE_CLK	DO, PD	Used for external MIPI IC control	1.8 V
58	RFFE_DATA	DIO, PD	Used for external MIPI IC control	1.8 V

NOTE

RFFE_CLK and RFFE_DATA are reserved only for customization.

4.8. Configuration Pins

The modules provide four configuration pins, which are defined as below.

4.8.1. EM160R-GL Configuration Pins

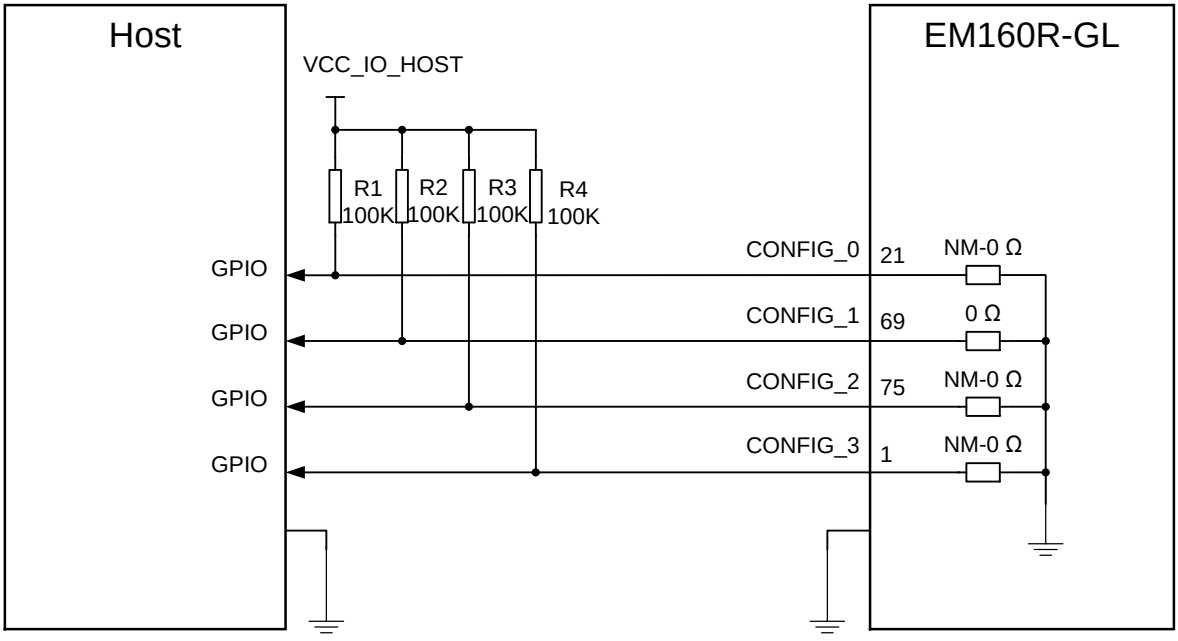
Table 32: List of EM160R-GL Configuration Pins

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	WWAN–USB3.0	2

Table 33: Pin Definition of EM160R-GL Configuration Pins

Pin No.	Pin Name	I/O	Description
21	CONFIG_0	DO	Not connected internally
69	CONFIG_1	DO	Connected to GND internally
75	CONFIG_2	DO	Not connected internally
1	CONFIG_3	DO	Not connected internally

The following figure shows a reference circuit for these four pins.



Note: The voltage level VCC_IO_HOST depends on the host side, and could be a 1.8 V or 3.3 V voltage level.

Figure 31: Recommended Circuit of EM160R-GL Configuration Pins

4.8.2. EM120R-GL Configuration Pins

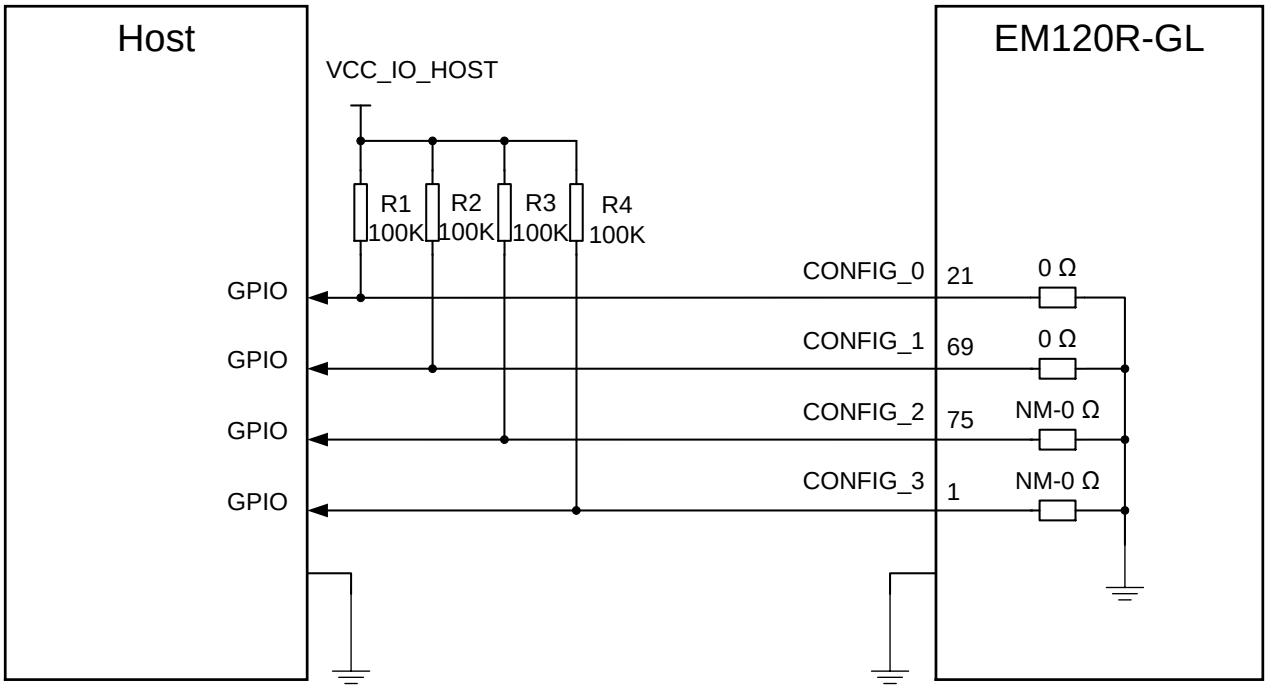
Table 34: List of EM120R-GL Configuration Pins

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
GND	GND	NC	NC	WWAN–USB3.0	2

Table 35: Pin Definition of EM120R-GL Configuration Pins

Pin No.	Pin Name	I/O	Description
21	CONFIG_0	DO	Connected to GND internally.
69	CONFIG_1	DO	Connected to GND internally
75	CONFIG_2	DO	Not connected internally
1	CONFIG_3	DO	Not connected internally

The following figure shows a reference circuit for these four pins.



Note: The voltage level VCC_IO_HOST depends on the host side, and could be a 1.8 V or 3.3 V voltage level.

Figure 32: Recommended Circuit of EM120R-GL Configuration Pins

5 RF Characteristics

5.1. Cellular Antenna Interfaces

EM120R-GL and EM160R-GL provide Main, Rx-diversity/GNSS and MIMO antenna connectors which are used to resist the fall of signals caused by high-speed movement and multipath effect. The impedance of antenna ports is 50 Ω.

EM160R-GL provides a Main, a Rx-diversity/GNSS and two MIMO antenna connectors.

EM120R-GL provides a Main and a Rx-diversity/GNSS antenna connectors.

5.1.1. Connector Definition

Table 36: EM120R-GL Connector Definition of Antenna Interfaces

Connector Name	I/O	Description	Comment
Main Antenna	AIO	Main Antenna interface: ● LTE: TRx ● WCDMA: TRx	50 Ω impedance
Rx-diversity/ GNSS Antenna	AI	Rx-diversity/GNSS Antenna interface: ● LTE: DRx ● WCDMA: DRx ● GNSS: L1	50 Ω impedance

Table 37: EM160R-GL Connector Definition of Antenna Interfaces

Connector Name	I/O	Description	Comment
Main Antenna	AIO	Main Antenna interface: ● LTE: TRx ● WCDMA: TRx	50 Ω impedance
Rx-diversity/ GNSS Antenna	AI	Rx-diversity/GNSS Antenna interface: ● LTE: DRx ● WCDMA: DRx	50 Ω impedance

		• GNSS: L1	
MIMO1 Antenna	AI	MIMO1 Antenna interface: • LTE: MHB_MIMO1	50 Ω impedance
MIMO2 Antenna	AI	MIMO2 Antenna interface: • LTE: MHB_MIMO2	50 Ω impedance

5.1.2. Operating Frequency

Table 38: Operating Frequencies of EM120R-GL&EM160R-GL

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B6	830–840	875–885	MHz
WCDMA B8	880–915	925–960	MHz
WCDAM B19	830–845	875–890	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B14	788–798	758–768	MHz

LTE-FDD B17	704–716	734–746	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B29 [1)]	-	717–728	MHz
LTE-FDD B30	2305–2315	2350–2360	MHz
LTE-FDD B32 [1)]	-	1452–1496	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz
LTE-TDD B42	3400–3600	3400–3600	MHz
LTE-TDD B43	3600–3800	3600–3800	MHz
LTE-TDD B46 [1)]	-	5150–5925	MHz
LTE-TDD B48	3550–3700	3550–3700	MHz
LTE-FDD B66	1710–1780	2110–2200	MHz

NOTE

[1)] LTE-FDD B29/32 and LTE-TDD B46 support Rx only and are only for secondary component carrier.

5.1.3. Receiving Sensitivity

Table 39: EM120R-GL&EM160R-GL Dual-Antenna Conducted Receiving Sensitivity

Frequency Bands	RX Sensitivity [1] (Typical) (dBm)	3GPP (dBm)	Comment [2]
WCDMA B1	-110.5	-106.7	
WCDMA B2	-110	-104.7	
WCDMA B3	-111	-103.7	
WCDMA B4	-110.5	-106.7	
WCDMA B5	-112	-104.7	
WCDMA B6	-111	-106.7	
WCDMA B8	-111	-103.7	
WCDMA B19	-111	-106.7	
LTE-FDD B1	-100.7	-96.3	10 MHz
LTE-FDD B2	-100.3	-94.3	10 MHz
LTE-FDD B3	-100.3	-93.3	10 MHz
LTE-FDD B4	-100.6	-96.3	10 MHz
LTE-FDD B5	-101.7	-94.3	10 MHz
LTE-FDD B7	-99.4	-94.3	10 MHz
LTE-FDD B8	-101.3	-93.3	10 MHz
LTE-FDD B12	-102.3	-93.3	10 MHz
LTE-FDD B13	-102.2	-93.3	10 MHz
LTE-FDD B14	-101.8	-93.3	10 MHz
LTE-FDD B17	-102.3	-93.3	10 MHz
LTE-FDD B18	-102	-96.3	10 MHz
LTE-FDD B19	-102	-96.3	10 MHz
LTE-FDD B20	-101.8	-93.3	10 MHz

LTE-FDD B25	-100.3	-92.8	10 MHz
LTE-FDD B26	-101.9	-93.8	10 MHz
LTE-FDD B28	-101.6	-94.8	10 MHz
LTE-FDD B29 3)	-101	-93.3	10 MHz
LTE-FDD B30	-99.5	-95.3	10 MHz
LTE-FDD B32 3)	-99	-96.3	10 MHz
LTE-TDD B38	-100.1	-96.3	10 MHz
LTE-TDD B39	-100.5	-96.3	10 MHz
LTE-TDD B40	-99.2	-96.3	10 MHz
LTE-TDD B41	-99.7	-94.3	10 MHz
LTE-TDD B42	-100.7	-95.0	10 MHz
LTE-TDD B43	-100.7	-95.0	10 MHz
LTE-TDD B46 3)	-96.5	-88.5	20 MHz
LTE-TDD B48	-100.6	-95.0	10 MHz
LTE-FDD B66	-100.4	-95.8	10 MHz

NOTES

1. 1) Rx Sensitivity values are measured in dual antennas condition (Primary + Diversity). For single primary antenna (without Diversity), the sensitivity will drop around 3 dBm for each LTE band.
2. 2) The RB configure follows 3GPP specification.
3. 3) The test results are based on CA_2A-29A, CA_20A-32A and CA_46A-66A.

Table 40: EM160R-GL Four-Antenna Conducted Receiving Sensitivity

Frequency Bands	RX Sensitivity 1) (Typical) (dBm)	3GPP (dBm)	Comment 2)
LTE-FDD B1	-103.5	-99	10 MHz
LTE-FDD B2	-103	-97	10 MHz
LTE-FDD B3	-102.8	-96	10 MHz

LTE-FDD B4	-103	-99	10 MHz
LTE-FDD B7	-102.3	-97	10 MHz
LTE-FDD B25	-103	-95.5	10 MHz
LTE-FDD B30	-102.5	-98	10 MHz
LTE-FDD B32 3)	-102	-	10 MHz
LTE-TDD B38	-102.5	-	10 MHz
LTE-TDD B39	-102.5	-99	10 MHz
LTE-TDD B40	-102.2	-99	10 MHz
LTE-TDD B41	-102	-97	10 MHz
LTE-FDD B66	-103	-98.5	10 MHz

NOTES

1. 1) Rx Sensitivity values are measured in four antennas condition (Primary + Diversity + MIMO1 + MIMO2). If only use dual antennas (Primary + Diversity), the sensitivity will drop about 3 dBm for each band of LTE.
2. 2) The RB configure follows 3GPP specification.
3. 3) The test result is based on CA_20A-32A.

5.1.4. Output Power

Table 41: EM120R-GL&EM160R-GL RF Output Power of PCIe Only Version

Frequency Bands	Modulation	Max.	Min.	Comment
WCDMA B1	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B2	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B3	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B4	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B5	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B6	BPSK	24 dBm +1/-3 dB	< -50 dBm	

WCDMA B8	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B19	BPSK	24 dBm +1/-3 dB	< -50 dBm	
LTE-FDD B1	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B2	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B3	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B4	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B5	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B7	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B8	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B12	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B13	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B14	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B17	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B18	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B19	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B20	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B25	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B26	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B28	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B30	QPSK	22 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B38	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B39	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B40	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B41	QPSK	23 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B41 HPUE	QPSK	25.5 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB

LTE-TDD B42	QPSK	21 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B43	QPSK	21 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B48	QPSK	21 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B66	QPSK	24 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB

Table 42: EM120R-GL&EM160R-GL RF Output Power of USB Version

Frequency Bands	Modulation	Max.	Min.	Comment
WCDMA B1	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B2	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B3	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B4	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B5	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B6	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B8	BPSK	24 dBm +1/-3 dB	< -50 dBm	
WCDMA B19	BPSK	24 dBm +1/-3 dB	< -50 dBm	
LTE-FDD B1	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B2	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B3	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B4	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B5	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B7	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B8	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B12	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B13	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B14	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B17	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB

LTE-FDD B18	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B19	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B20	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B25	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B26	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B28	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B30	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B38	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B39	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B40	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B41	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B41 HPUE	QPSK	25.5 dBm +1/-2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B42	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B43	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-TDD B48	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB
LTE-FDD B66	QPSK	23 dBm ±2 dB	< -40 dBm	10 MHz, 1RB

5.2. GNSS Antenna Interface

5.2.1. General Description

EM120R-GL and EM160R-GL include a fully integrated global navigation satellite system solution that supports Gen9-VT of Qualcomm (GPS, GLONASS, BeiDou/COMPASS and Galileo).

The module supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the module GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, see ***document [4]***.

5.2.2. GNSS Frequency

Table 43: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo	1575.42 ±1.023	MHz
GLONASS	1601.65 ±4.15	MHz
BeiDou/COMPASS	1561.098 ±2.046	MHz

5.2.3. GNSS Performance

Table 44: EM120R-GL&EM160R-GL GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-158	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	31.13	s
		XTRA enabled	17.87	s
	Warm start @ open sky	Autonomous	26.59	s
		XTRA enabled	7.07	s
	Hot start @ open sky	Autonomous	2.12	s
		XTRA enabled	2.6	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	2	m

NOTES

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after the loss of lock.

3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.3. Antenna Connectors

5.3.1. Antenna Connector Location

The antenna connector locations are shown below.

Figure 33: Antenna Connectors on the EM160R-GL Module

Figure 34: Antenna Connectors on the EM120R-GL Module

5.3.2. Antenna Connector Size

Standard 2 mm × 2 mm receptacle antenna connectors are mounted for convenient antenna connection. The antenna connector's PN is IPEX 20449-001E, and the connector dimensions are illustrated as below:

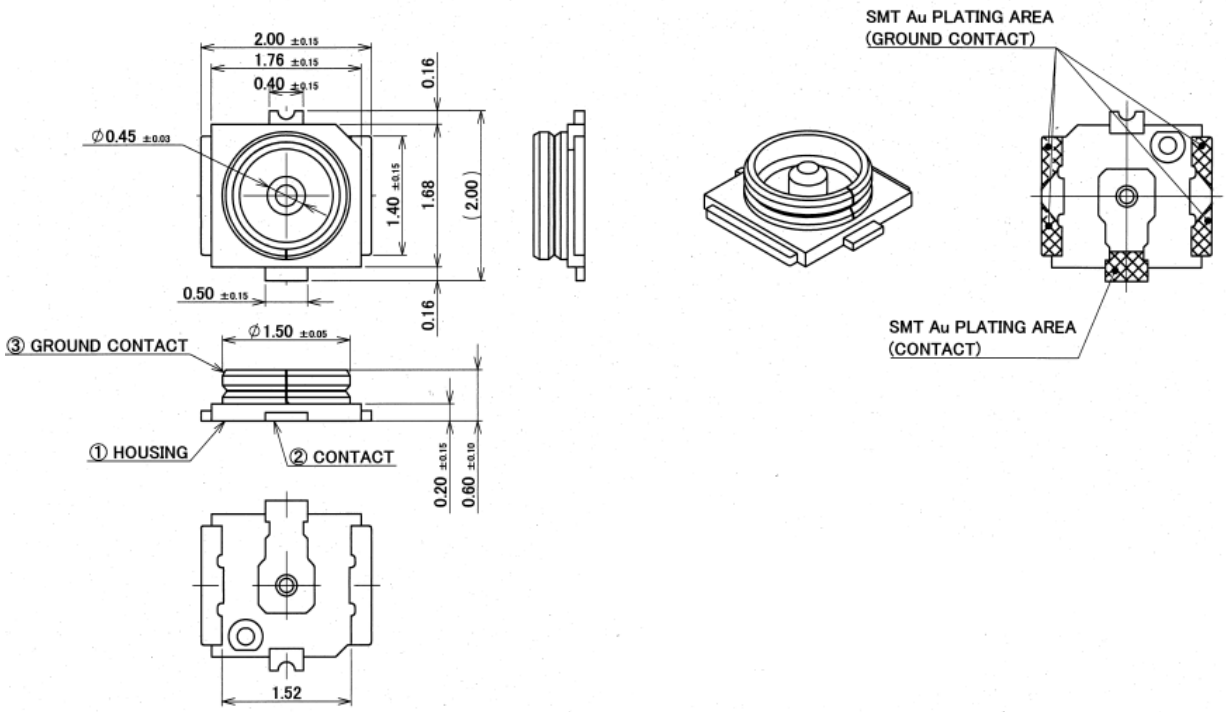


Figure 35: EM120R-GL&EM160R-GL RF Connector Dimensions (Unit: mm)

Table 45: Major Specifications of the RF Connectors

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.4 (3–6 GHz)

5.3.3. Antenna Connector Installation

The 2 mm × 2 mm connector dimensions are illustrated below:

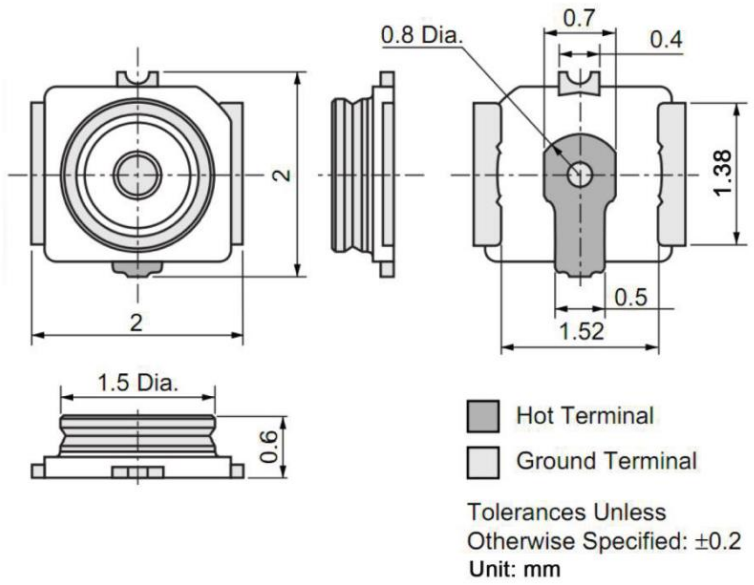


Figure 36: EM120R-GL&EM160R-GL RF Connector Dimensions (Unit: mm)

The receptacle RF connector used in conjunction with the module will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø 0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a Ø 1.13 mm coaxial cable.

The following figure shows the specifications of mating plugs using Ø 0.81 mm coaxial cables.

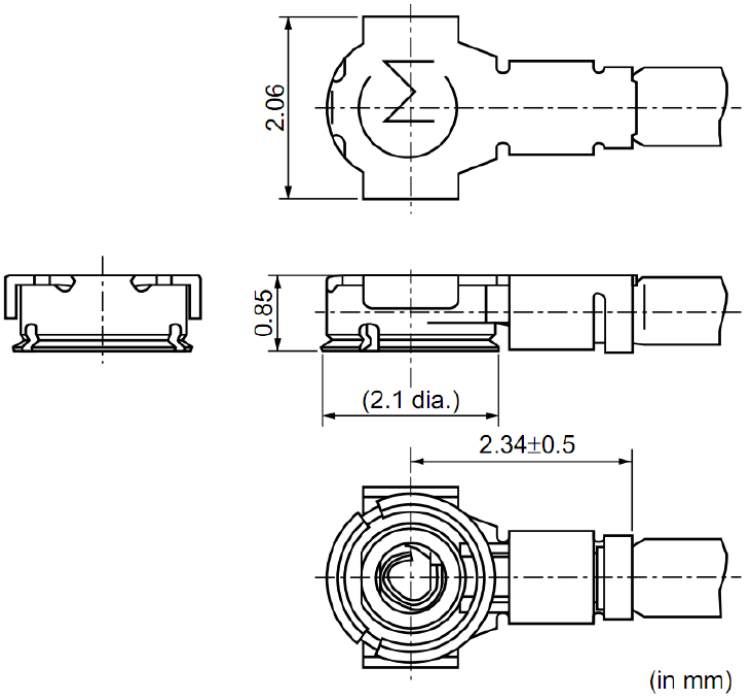


Figure 37: Specifications of Mating Plugs Using Ø 0.81 mm Coaxial Cables

The following figure illustrates the connection between the receptacle RF connector on the module and the mating plug using a Ø 0.81 mm coaxial cable.

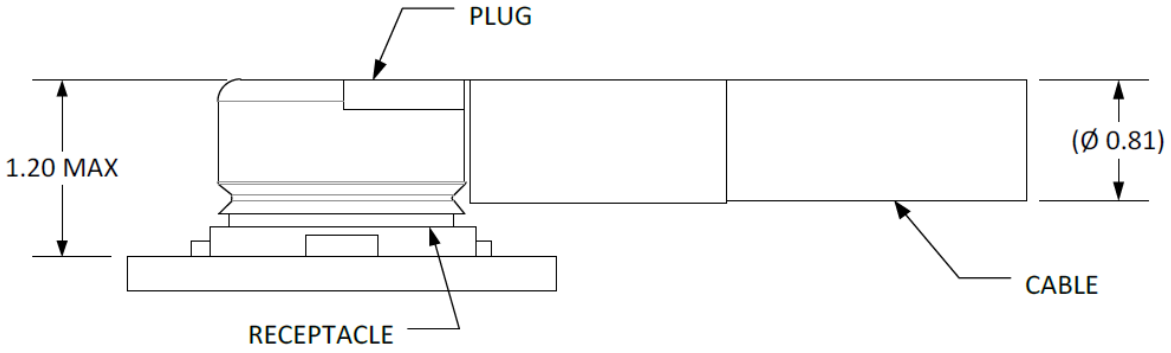


Figure 38: Connection between RF Connector and Mating Plug Using Ø 0.81 mm Coaxial Cable

The following figure illustrates the connection between the receptacle RF connector on the module and the mating plug using a Ø 1.13 mm coaxial cable.

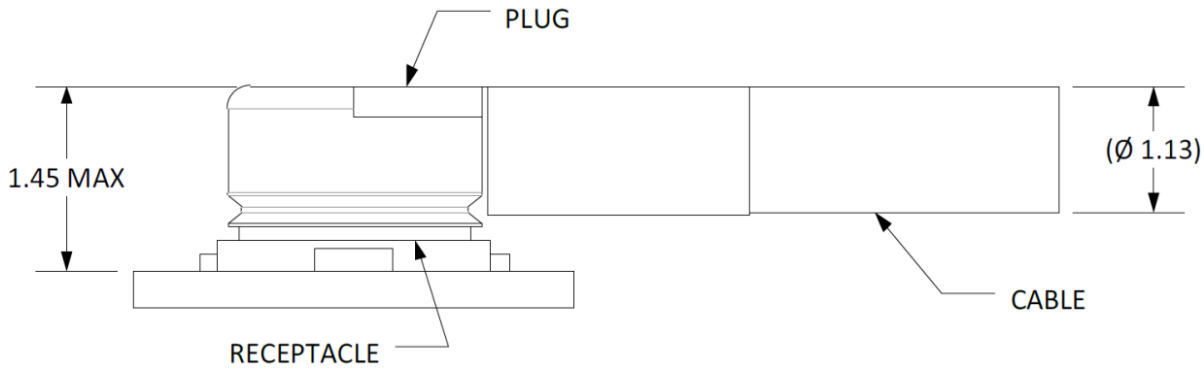


Figure 39: Connection between RF Connector and Mating Plug Using Ø 1.13 mm Coaxial Cable

5.4. Antenna Requirements

Table 46: Antenna Requirements of EM160R-GL

Type	Requirements	Supported Bands
Main Antenna (Tx/Rx)	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1710–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66 **WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19
Rx-diversity/ GNSS Antenna	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66 **WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19 **GNSS:**

		GPS; GLONASS; BeiDou/COMPASS; Galileo
MIMO1 Antenna (Rx)	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B7/B25/ B30/B32/B38/B39/B40/B41/B66
MIMO2 Antenna (Rx)	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B7/B25/ B30/B32/B38/B39/B40/B41/B66

Table 47: Antenna Requirements of EM120R-GL

Type	Requirements	Supported Bands
Main Antenna (Tx/Rx)	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1710–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66 **WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19
Rx-diversity/ GNSS Antenna	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66

	(699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19 **GNSS:** GPS; GLONASS; BeiDou/COMPASS; Galileo

NOTE

Active GNSS antenna is not supported.

6 Electrical Characteristics and Reliability

6.1. Power Supply Requirements

The typical input voltage of the module is 3.7 V. The following table shows the power supply requirements of the module.

Table 48: Power Supply Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.135	3.7	4.4	V
Voltage Ripple	-	-	30	100	mV
Voltage Drop	-	-	-	165	mV

6.2. Current Consumption

6.2.1. PCIe Only Version

Table 49: EM120R-GL&EM160R-GL Current Consumption (PCIe Only Version, 3.3 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	66	μA
Sleep State	**AT+CFUN=0** @ Modem standby	2.38	mA
	WCDMA PF = 64 @ Modem standby	3.36	mA
	LTE-FDD PF = 64 @ Modem standby	3.77	mA

	LTE-TDD PF = 64 @ Modem standby	3.71	mA
Idle State	WCDMA PF = 64(B1 CH10700 Modem standby)	9.65	mA
	WCDMA PF = 64(B1 CH10700 PCIe Active)	14.69	mA
	LTE-FDD PF = 64(B1 CH300 Modem standby)	9.4	mA
	LTE-FDD PF = 64(B1 CH300 PCIe Active)	15.15	mA
	LTE-TDD PF = 64(B38 CH38000 Modem standby)	10.19	mA
	LTE-TDD PF = 64(B38 CH38000 PCIe Active)	15.75	mA
WCDMA Data Transfer (GNSS Off)	WCDMA B1 HSDPA CH10700 @ 23.57 dBm	654.21	mA
	WCDMA B1 HSUPA CH10700 @ 23.54 dBm	646.25	mA
	WCDMA B2 HSDPA CH9800 @ 23.25 dBm	561.06	mA
	WCDMA B2 HSUPA CH9800 @ 23.29 dBm	588.27	mA
	WCDMA B3 HSDPA CH1338 @ 23.07 dBm	595.17	mA
	WCDMA B3 HSUPA CH1338 @ 23.26 dBm	598.19	mA
	WCDMA B4 HSDPA CH1638 @ 23.43 dBm	642.02	mA
	WCDMA B4 HSUPA CH1638 @ 23.5 dBm	661.27	mA
	WCDMA B5 HSDPA CH4407 @ 22.62 dBm	511.57	mA
	WCDMA B5 HSUPA CH4407 @ 22.8 dBm	508.58	mA
	WCDMA B6 HSDPA CH4400 @ 22.66 dBm	515.95	mA
	WCDMA B6 HSUPA CH4400 @ 22.83 dBm	532.86	mA
	WCDMA B8 HSDPA CH3012 @ 22.75 dBm	566.86	mA
	WCDMA B8 HSUPA CH3012 @ 22.93 dBm	570.14	mA
	WCDMA B19 HSDPA CH738 @ 22.52 dBm	507.47	mA
	WCDMA B19 HSUPA CH738 @ 22.34 dBm	489.19	mA
LTE Data Transfer (GNSS Off)	LTE-FDD B1 CH300 @ 24.81 dBm	919.73	mA
	LTE-FDD B2 CH900 @ 24.86 dBm	785.26	mA

	LTE-FDD B3 CH1575 @ 24.35 dBm	784	mA
	LTE-FDD B4 CH2175 @ 24.79 dBm	895.19	mA
	LTE-FDD B5 CH2525 @ 24.64 dBm	707.23	mA
	LTE-FDD B7 CH3100 @ 23.62 dBm	902.96	mA
	LTE-FDD B8 CH3625 @ 24.91 dBm	810.75	mA
	LTE-FDD B12 CH5095 @ 24.64 dBm	683.56	mA
	LTE-FDD B13 CH5230 @ 24.39 dBm	705.3	mA
	LTE-FDD B14 CH5330 @ 24.54 dBm	680.13	mA
	LTE-FDD B17 CH5790 @ 24.57 dBm	679.79	mA
	LTE-FDD B18 CH5925 @ 24.83 dBm	716.38	mA
	LTE-FDD B19 CH6075 @ 24.99 dBm	662.82	mA
	LTE-FDD B20 CH6300 @ 24.32 dBm	673.72	mA
	LTE-FDD B25 CH8365 @ 24.68 dBm	752.8	mA
	LTE-FDD B26 CH8865 @ 24.4 dBm	676.59	mA
	LTE-FDD B28A CH9360 @ 24.62 dBm	706.65	mA
	LTE-FDD B28B CH9510 @ 24.35 dBm	694.21	mA
	LTE-FDD B30 CH9820 @ 22.17 dBm	917.82	mA
	LTE-FDD B66 CH132322 @ 24.73 dBm	865.75	mA
	LTE-TDD B38 CH38000 @ 24.27 dBm	550.65	mA
	LTE-TDD B39 CH38450 @ 24.4 dBm	367.78	mA
	LTE-TDD B40 CH39150 @ 24.22 dBm	528.9	mA
	LTE-TDD B41 CH40620 @ 25.29 dBm	649.66	mA
	LTE-TDD B42 CH42590 @ 20.99 dBm	300.36	mA
	LTE-TDD B43 CH44590 @ 21.61 dBm	307.41	mA
	LTE-TDD B48 CH55590 @ 21.88 dBm	305.05	mA

WCDMA Voice Call	WCDMA B1 CH10700 @ 24.52 dBm	739.17	mA
	WCDMA B2 CH9800 @ 24.25 dBm	648.81	mA
	WCDMA B3 CH1338 @ 24.18 dBm	680.93	mA
	WCDMA B4 CH1638 @ 24.41 dBm	788.8	mA
	WCDMA B5 CH4407 @ 23.85 dBm	577.69	mA
	WCDMA B6 CH4400 @ 23.84 dBm	578.14	mA
	WCDMA B8 CH3012 @ 23.89 dBm	635.27	mA
	WCDMA B19 CH738 @ 23.83 dBm	566.84	mA

6.2.2. USB Version

Table 50: EM120R-GL&EM160R-GL Current Consumption (USB Only Version, 3.7 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	66	μA
Sleep State	**AT+CFUN=0** @ USB Suspend	1.78	mA
	WCDMA PF = 64 @ USB Suspend	2.35	mA
	LTE-FDD PF = 64 @ USB Suspend	2.96	mA
	LTE-TDD PF = 64 @ USB Suspend	2.73	mA
Idle State	WCDMA PF = 64 (B1 CH10700 USB Disconnect)	TBD	mA
	WCDMA PF = 64 (B1 CH10700 USB Connect)	20.16	mA
	LTE-FDD PF = 64 (B1 CH300 USB Disconnect)	TBD	mA
	LTE-FDD PF = 64 (B1 CH300 USB Connect)	24.69	mA
	LTE-TDD PF = 64 (B38 CH38000 USB Disconnect)	TBD	mA
	LTE-TDD PF = 64 (B38 CH38000 USB Connect)	24.48	mA
WCDMA Data Transfer (GNSS Off)	WCDMA B1 HSDPA CH10700 @ 23.21 dBm	555.22	mA
	WCDMA B1 HSUPA CH10700 @ 23.12 dBm	544.69	mA

	WCDMA B2 HSDPA CH9800 @ 23.43 dBm	554.48	mA
	WCDMA B2 HSUPA CH9800 @ 23.45 dBm	546.39	mA
	WCDMA B3 HSDPA CH1338 @ 23.53 dBm	549.06	mA
	WCDMA B3 HSUPA CH1338 @ 23.23 dBm	520.05	mA
	WCDMA B4 HSDPA CH1638 @ 21.97 dBm	507.84	mA
	WCDMA B4 HSUPA CH1638 @ 21.96 dBm	500.32	mA
	WCDMA B5 HSDPA CH4407 @ 21.9 dBm	423.69	mA
	WCDMA B5 HSUPA CH4407 @ 21.42 dBm	408.88	mA
	WCDMA B6 HSDPA CH4400 @ 21.9 dBm	402.89	mA
	WCDMA B6 HSUPA CH4400 @ 21.4 dBm	394.32	mA
	WCDMA B8 HSDPA CH3012 @ 23.32 dBm	523.66	mA
	WCDMA B8 HSUPA CH3012 @ 23.3 dBm	526.95	mA
	WCDMA B19 HSDPA CH738 @ 21.89 dBm	396.31	mA
	WCDMA B19 HSUPA CH738 @ 21.95 dBm	408.61	mA
LTE Data Transfer (GNSS Off)	LTE-FDD B1 CH300 @ 23.46 dBm	643.25	mA
	LTE-FDD B2 CH900 @ 23.4 dBm	590.75	mA
	LTE-FDD B3 CH1575 @ 23.25 dBm	617.12	mA
	LTE-FDD B4 CH2175 @ 23.18 dBm	627.14	mA
	LTE-FDD B5 CH2525 @ 22.91 dBm	462.72	mA
	LTE-FDD B7 CH3100 @ 23.05 dBm	767.25	mA
	LTE-FDD B8 CH3625 @ 23.16 dBm	521.65	mA
	LTE-FDD B12 CH5095 @ 23.09 dBm	458.28	mA
	LTE-FDD B13 CH5230 @ 22.83 dBm	476.31	mA
	LTE-FDD B14 CH5330 @ 22.8 dBm	483.46	mA
	LTE-FDD B17 CH5790 @ 23.04 dBm	474.84	mA

	LTE-FDD B18 CH5925 @ 23.04 dBm	493.84	mA
	LTE-FDD B19 CH6075 @ 23.07 dBm	458.69	mA
	LTE-FDD B20 CH6300 @ 22.94 dBm	480.64	mA
	LTE-FDD B25 CH8365 @ 23.4 dBm	550.14	mA
	LTE-FDD B26 CH8865 @ 23.14 dBm	502.43	mA
	LTE-FDD B28A CH9360 @ 22.42 dBm	492.22	mA
	LTE-FDD B28B CH9510 @ 22.99 dBm	493.8	mA
	LTE-FDD B30 CH9820 @ 23.52 dBm	782.27	mA
	LTE-FDD B66 CH132322 @ 22.74 dBm	604.55	mA
	LTE-TDD B38 CH38000 @ 23.47 dBm	380.28	mA
	LTE-TDD B39 CH38450 @ 23.37 dBm	305.56	mA
	LTE-TDD B40 CH39150 @ 23.09 dBm	426.58	mA
	LTE-TDD B41 CH40620 @ 22.85 dBm	371.09	mA
	LTE-TDD B42 CH42590 @ 23.07 dBm	340.09	mA
	LTE-TDD B43 CH44590 @ 22.56 dBm	337.44	mA
	LTE-TDD B48 CH55590 @ 23.28 dBm	324.22	mA
WCDMA Voice Call	WCDMA B1 CH10700 @ 23.16 dBm	592.83	mA
	WCDMA B2 CH9800 @ 23.46 dBm	553.09	mA
	WCDMA B3 CH1338 @ 23.56 dBm	552.49	mA
	WCDMA B4 CH1638 @ 23.09 dBm	581.05	mA
	WCDMA B5 CH4407 @ 23.39 dBm	456.58	mA
	WCDMA B6 CH4400 @ 22.99 dBm	445.65	mA
	WCDMA B8 CH3012 @ 23.47 dBm	535.81	mA
	WCDMA B19 CH738 @ 22.98 dBm	438.75	mA

6.3. Digital I/O Characteristic

Table 51: Logic Levels of Digital I/O (1.8 V)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.65	2.1	V
V_{IL}	Input low voltage	-0.3	0.54	V
V_{OH}	Output high voltage	1.3	1.8	V
V_{OL}	Output low voltage	0	0.4	V

Table 52: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.4	V

Table 53: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.4	V

6.4. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

Table 54: Electrostatic Discharge Characteristics (Temperature: 25 ºC, Humidity: 40 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VCC, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.5. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 55: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
VCC	-0.3		4.7	V

6.6. Operating and Storage Temperatures

Table 56: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [1)]	-25	+25	+75	ºC
Extended Temperature Range [2)]	-40	-	+85	ºC

Storage temperature Range	-40	-	+90	ºC

NOTES

1. [1)] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module meets 3GPP specifications.
2. [2)] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

7 Mechanical Dimensions and Packaging

This chapter mainly describes mechanical dimensions and packaging specifications of EM120R-GL and EM160R-GL. All dimensions are measured in mm, and the tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

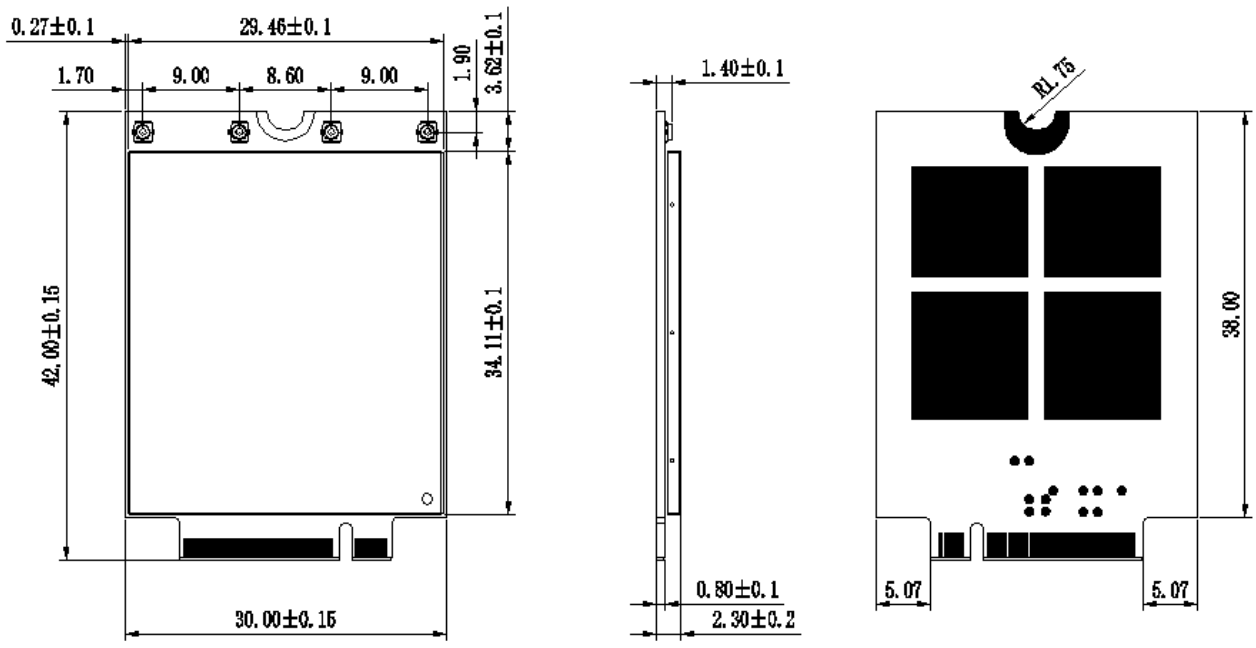


Figure 40: Mechanical Dimensions of the Module (Unit: mm)

7.2. Top and Bottom Views of the Module

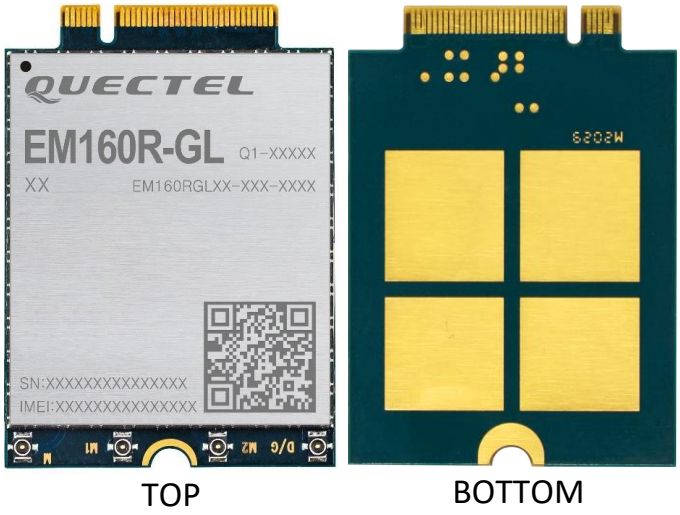


Figure 41: EM160R-GL Top View and Bottom View

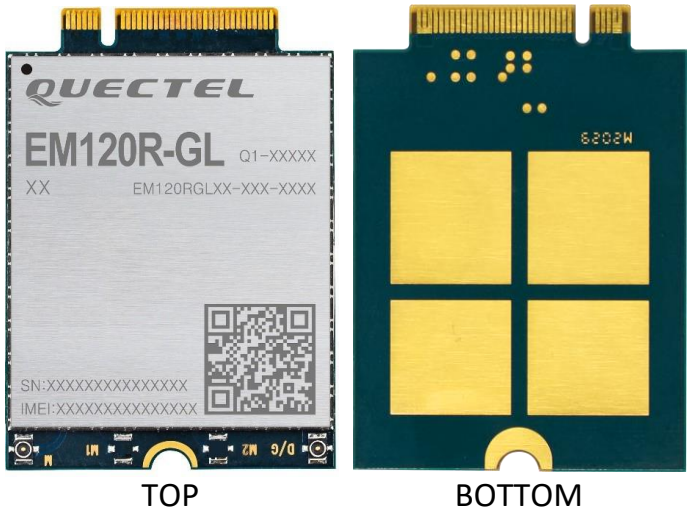


Figure 42: EM120R-GL Top View and Bottom View

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7.3. M.2 Connector

EM120R-GL and EM160R-GL adopts a standard PCI Express M.2 connector which compiles with the directives and standards listed in *PCI Express M.2 Specification*.

7.4. Packaging

Modules are packaged in trays. The following figure shows the tray size.

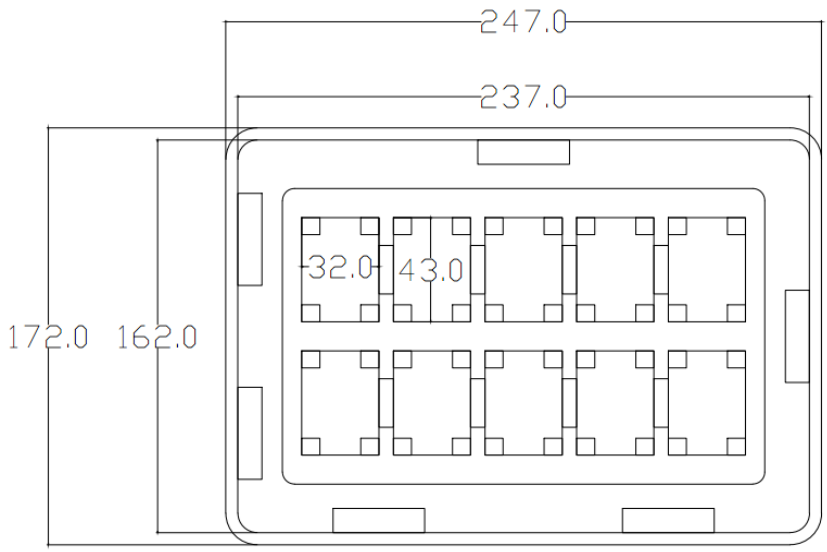


Figure 43: Tray Size (Unit: mm)

Each tray contains 10 modules. The smallest package contains 100 modules. Tray packaging procedures are as below.

1. Use 10 trays to package 100 modules at a time (tray size: 247 mm × 172 mm).
2. Place an empty tray on the top of the 10-tray stack.
3. Fix the stack with masking tape in "#" shape as shown in the following figure.
4. Pack the stack with conductive bag, and then fix the bag with masking tape.
5. Place the list of IMEI No. into a small carton.
6. Seal the carton and then label the seal with sealing sticker (small carton size: 250 mm × 175 mm × 128 mm).

Figure 44: Tray Packaging Procedure

8 Appendix References

Table 57: Related Documents

SN.	Document Name	Description
[1]	Quectel_EM120R-GL&EM160R-GL_CA_Feature	EM120R-GL&EM160R-GL CA Feature
[2]	Quectel_PCIe_Card_EVB_User_Guide	The PCIE-CARD-EVB user guide
[3]	Quectel_EG512R&EM1x0R_Series_AT_Commands_Manual	AT commands manual for EG512R and EM1x0R-GL series
[4]	Quectel_EM1x0R-GL&EG512R_Series_GNSS_Application_Note	The GNSS application note for EM1x0R-GL&EG512R_Series

Table 58: Terms and Abbreviations

Abbreviation	Description
BIOS	Basic Input Output System
bps	Bit Per Second
BPSK	Binary Phase Shift Keying
CPE	Customer Premise Equipment
COEX	Coexistence
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DPR	Dynamic Power Reduction
DRX	Discontinuous Reception
DRx	Diversity Receive
EIRP	Equivalent Isotropically Radiated Power

ESD	Electrostatic Discharge
FDD	Frequency Division Duplexing
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
kbps	Kilo Bits Per Second
LAA	License Assisted Access
LED	Light Emitting Diode
LTE	Long Term Evolution
Mbps	Mega Bits Per Second
ME	Mobile Equipment
MIMO	Multiple-Input Multiple-Output
MLCC	Multiplayer Ceramic Chip Capacitor
MO	Mobile Originated
MSB	Most Significant Bit
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PME	Power Management Event

PPP	Point-to-Point Protocol
QPSK	Quadrature Phase Shift Keying
RB	Resource Block
RF	Radio Frequency
RFFE	RF Front-End
R.H	Relative humility
Rx	Receive
SAR	Specific Absorption Rate
SMS	Short Message Service
TCP	Transmission Control Protocol
TRx	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UL	Uplink
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	Input High Voltage Level
V_{IL}	Input Low Voltage Level
V_{OH}	Output High Voltage Level
V_{OL}	Output Low Voltage Level
WCDMA	Wideband Code Division Multiple Access