BC660K-GL

Hardware Design

NB-IoT Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2020-09-30	Clifton HE/ Ellison WANG/ Randy LI	Creation of the document
1.0	2021-01-12	Clifton HE/ Ellison WANG/ Randy LI	First official release

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1 Introduction

This document provides information on the functional features, interface specifications, as well as electrical and mechanical details of the BC660K-GL module. Consult this document to learn about the air interface, hardware interface, external application reference designs and other related information of the module.

This document, coupled with application notes and user guides, makes it easy to design and set up applications with BC660K-GL.

2 Product Concept

2.1. General Description

BC660K-GL is a high-performance NB-IoT module with extremely low power consumption. It is designed to communicate with infrastructures of mobile network operators through NB-IoT radio protocols 3GPP Rel-13 and Rel-14. BC660K-GL supports a broad range of frequency bands as listed below.

Table 1: Frequency Bands of BC660K-GL

Mode	BC660K-GL
H-FDD	B1/B2/B3/B4/B5/B8/B12/B13/B14/B17/B18/B19/B20/B25/B28/B66/B70/B85

BC660K-GL is an SMD type module with LCC and LGA package, and has an ultra-compact profile of 17.7 mm × 15.8 mm × 2.0 mm, which makes it easily embedded into size-constrained applications and provide reliable connectivity with the applications.

BC660K-GL provides abundant external interfaces (UART, ADC, USIM, etc.) and protocol stacks (UDP/TCP/LwM2M*/MQTT*, etc.), which facilitates the module's application.

The module's compact form factor, ultra-low power consumption and extended temperature range makes it one of the best choices for a wide range of IoT application, such as smart metering, bike sharing, smart wearables, smart parking, smart city, home appliances, security and asset tracking, agricultural and environmental monitoring, etc. It also provides a complete range of SMS* and data transmission services to meet various user demands.

The module fully complies with the RoHS directive of the European Union.

NOTE

"*" means under development.

2.2. Key Features

The following table describes the detailed features of BC660K-GL module.

Table 2: Key Features of BC660K-GL

Item	Details
Power Supply	● Supply voltage: 2.2–4.3 V ● Typical supply voltage: 3.3 V
Power Saving	Typical power consumption: 800 nA
Frequency Bands	**LTE Cat NB2:** B1/B2/B3/B4/B5/B8/B12/B13/B14/B17/B18/B19/B20/B25/B28/B66/B70/B85
Transmitting Power	23 dBm ±2 dB
USIM Interface	Support 1.8/3.0 V USIM card
UART Interfaces	**Main UART Port:** ● Used for AT command communication and data transmission, where the baud rate is 115200 bps by default. For more details, see ***Chapter 3.7.1***. ● Used for firmware upgrade, where the baud rate is 921600 bps by default. **Debug UART Port:** ● Used for debugging ● Default baud rate: 6 Mbps
Network Protocols	UDP/TCP/SNTP/LwM2M*/MQTT*/TLS*/DTLS*/SSL*
SMS*	● Text Mode ● PDU Mode
Data Transmission Features	● Single-tone (max): 25.5 kbps (DL)/16.7 kbps (UL) ● Multi-tone (max): 127 kbps (DL)/158.5 kbps (UL)
AT Commands	● 3GPP TS 27.005/3GPP TS 27.007 AT commands (3GPP Rel-13) ● Quectel enhanced AT commands
Firmware Update	● Upgrade firmware via main UART port ● Upgrade firmware via DFOTA
Real Time Clock	Supported
Physical Characteristics	● Size: (17.7 ±0.15) mm × (15.8 ±0.15) mm × (2.0 ±0.2) mm ● Weight: 1.0 ±0.2 g
Temperature Range	● Operating temperature range: -35 to +75 °C [1)] ● Extended temperature range: -40 to +85 °C [2)] ● Storage temperature range: -40 to +90 °C

Antenna Interface	50 Ω impedance control
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within operating temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module maintains functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of BC660K-GL and illustrates the major functional parts.

- RF Transceiver and Subsystem
- Baseband
- Power Management Unit
- Peripheral Interfaces

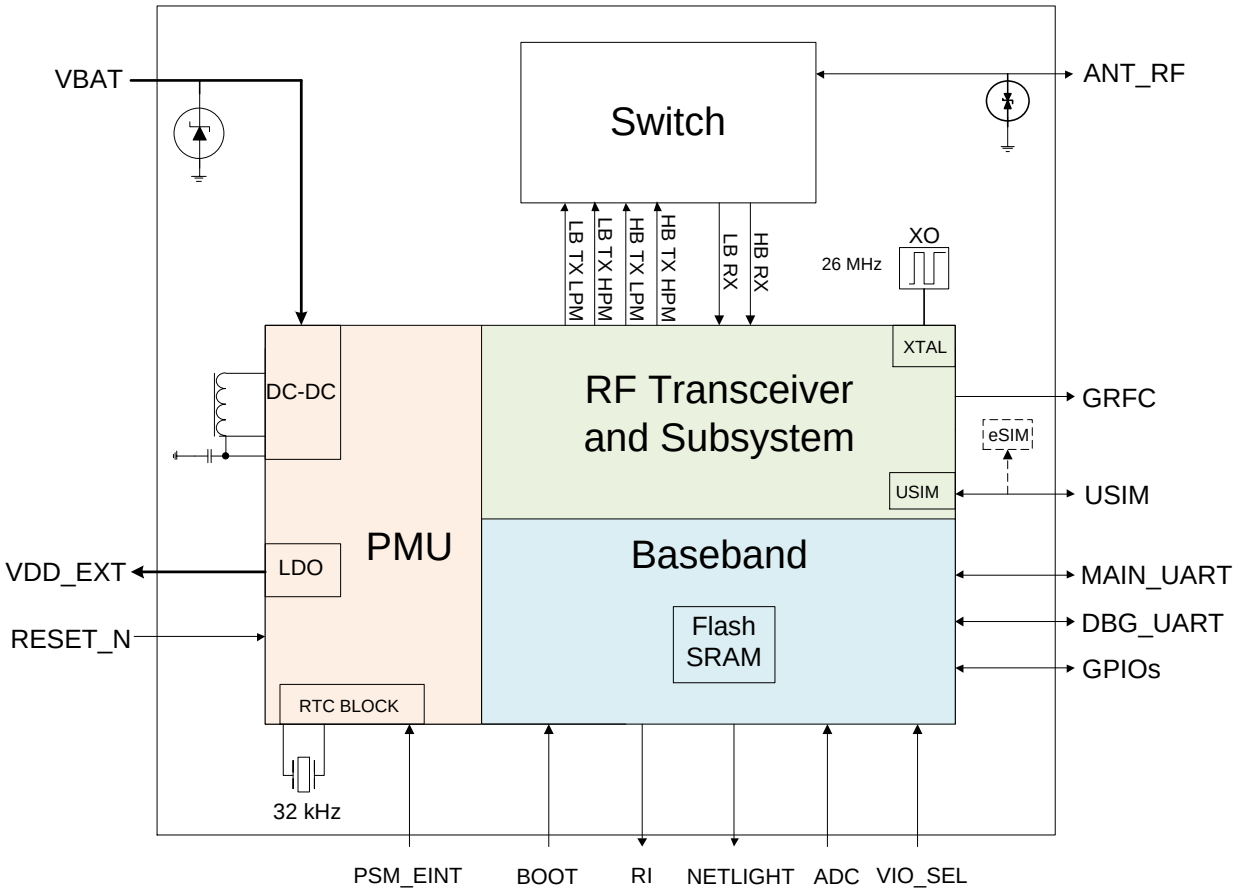


Figure 1: Functional Diagram

2.4. Evaluation Board

Quectel provides a complete set of development tools to facilitate the use and testing of BC660K-GL module. The development tool kit includes a TE-B board, a micro-USB cable, a rod antenna and other peripherals. For more details, see ***document [1]***.

3 Application Functions and Interfaces

BC660K-GL is equipped with 58 pins, including 44 LCC pins and 14 LGA pins. The subsequent chapters provide detailed descriptions of the following functions/pins/interfaces:

- Power Supply
- PSM_EINT
- RESET_N
- BOOT
- UART Interfaces
- USIM Interface
- ADC Interface
- RI Interface
- GPIO interfaces
- GRFC interfaces*
- NETLIGHT Interface*

NOTE

"*" means under development.

3.1. Pin Assignment

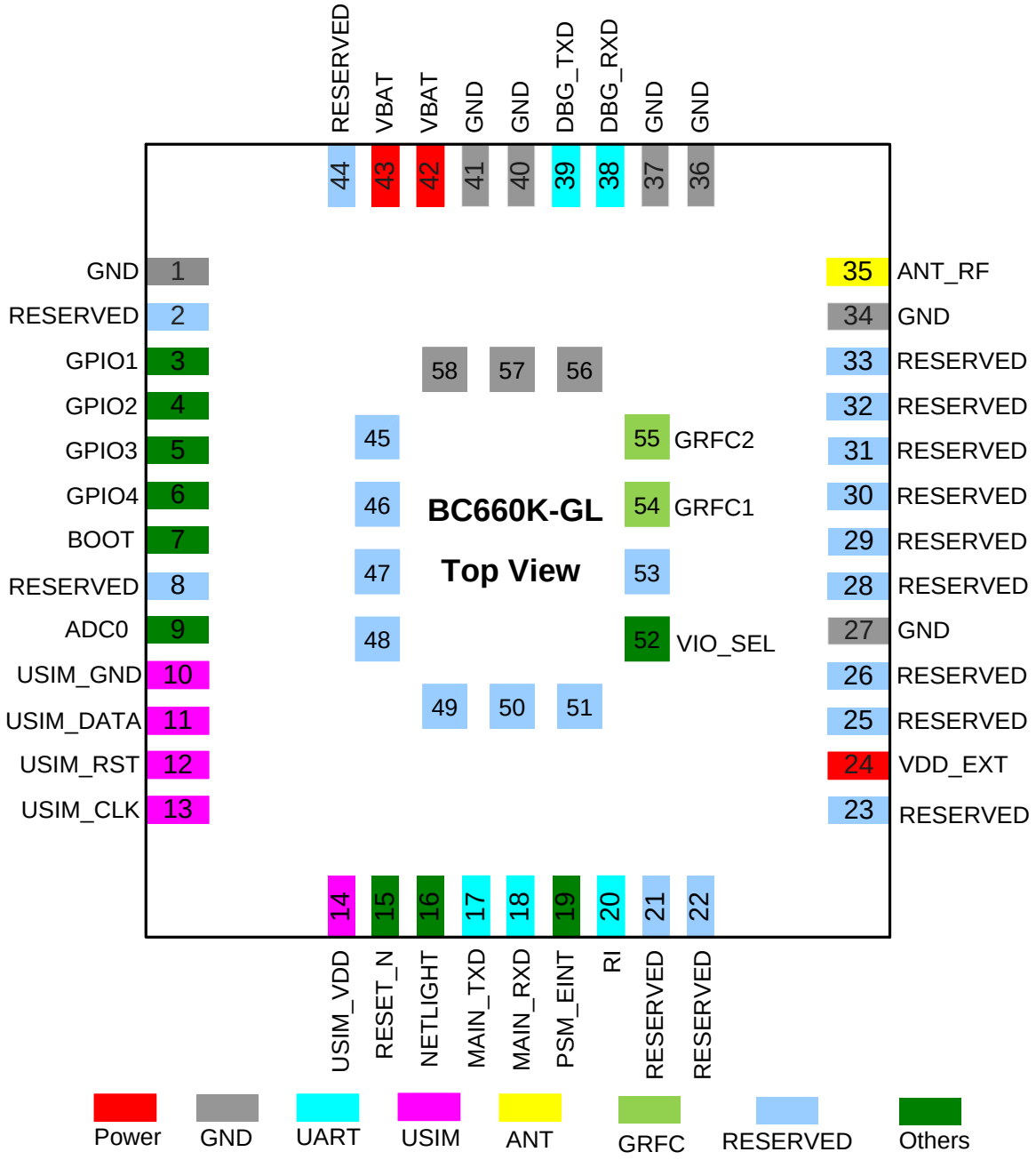


Figure 2: Pin Assignment

NOTE

Keep all reserved and unused pins unconnected.

3.2. Pin Description

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Power supply for the module	Vmax = 4.3 V Vmin = 2.2 V Vnom = 3.3 V	-
VDD_EXT	24	PO	1.8/3.3 V output power supply (Controlled by VIO_SEL, 1.8 V default)	Vnom = 1.8/3.3 V	No voltage output in Deep Sleep/Light Sleep mode. It is intended to supply power for the module's pull-up circuits, and is not recommended to be used as the power supply for external circuits.
GND	1, 27, 34, 36, 37, 40, 41, 56, 57, 58				-
BOOT interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BOOT	7	DI	Make the module enter	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	Active low.

			download mode		
Reset Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	15	DI	Reset the module	V_{IL}max = 0.42 V V_{IH}min = 1.33 V V_{IH}max = 2.2 V	Active low.
PSM_EINT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_EINT	19	DI	External interrupt pin dedicated to waking up the module from Deep/Light Sleep mode.	V_{IL}max = 0.42 V V_{IH}min = 1.33 V V_{IH}max = 2.2 V	Active on falling edge.
Network Status Indication*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NETLIGHT	16	DO	Indicate the module's network activity status	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	-
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	General-purpose analog to digital converter interface	Voltage range: 0–1.2 V	-
Main UART Port					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	18	DI	Main UART receive	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	-
MAIN_TXD	17	DO	Main UART transmit	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	VDD_EXT power domain.
Debug UART Port					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

DBG_RXD	38	DI	Debug UART receive	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	VDD_EXT power domain.
DBG_TXD	39	DO	Debug UART transmit	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	
RI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	20	DO	Ring indication	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	VDD_EXT power domain.
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_VDD	14	PO	USIM card power supply	Vnom = 1.8/3.0 V	-
USIM_CLK	13	DO	USIM card clock	V_{OL}max = 0.15 × USIM_VDD V_{OH}min = 0.8 × USIM_VDD	
USIM_RST	12	DO	USIM card reset	V_{OL}max = 0.15 × USIM_VDD V_{OH}min = 0.8 × USIM_VDD	
USIM_DATA	11	DIO	USIM card data	V_{IL}max = 0.2 × USIM_VDD V_{IH}min = 0.7 × USIM_VDD V_{OL}max = 0.15 × USIM_VDD V_{OH}min = 0.8 × USIM_VDD	
USIM_GND	10		Dedicated ground for USIM card	-	
Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_RF	35	DIO	RF antenna interface	-	50 Ω characteristic impedance
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	3	DIO	General-purpose input/output	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	VDD_EXT power domain. If unused, keep these pins open.
GPIO2	4	DIO	General-purpose input/output		
GPIO3	5	DIO	General-purpose input/output		

GPIO4	6	DIO	General-purpose input/output		
GRFC Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	54	DO	Generic RF controller	V_{OL}max = 0.27 V V_{OH}min = 1.44 V	1.8 V power domain. If unused, keep these pins open.
GRFC2	55	DO	Generic RF controller	V_{OL}max = 0.27 V V_{OH}min = 1.44 V	
Others					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIO_SEL	52	DI	IO Voltage selection	-	Control VDD_EXT voltage selection[1)]
Reserved Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	2, 8, 21–23, 25, 26, 28–33, 44–51, 53				Keep these pins open.

NOTES

1. Keep all reserved and unused pins unconnected.
2. [1)] When VIO_SEL is grounded and VBAT < 3.3 V, VDD_EXT = VBAT;
When VIO_SEL is grounded and VBAT ≥ 3.3 V, VDD_EXT = 3.3 V;
When VIO_SEL is floating, VDD_EXT = 1.8 V.
3. "*" means under development.

3.3. Operating Modes

The following table briefly describes the three working modes of the module.

Table 5: Application Processor (AP) Operating Modes

Mode	Description
Normal	In normal mode, the AP handles tasks such as AT command communication.
Idle	When all tasks are suspended, the AP enters idle mode.

Table 6: Modem Operating Modes

Mode	Description
Connected	The network is connected and the module supports data transmission. In such a case, the modem can switch to DRX/eDRX mode.
DRX/eDRX	The modem is in idle mode, and downlink data can be received during PTW only. In such a case, the modem can switch to PSM or connected mode.
PSM	In power saving mode, the modem is disconnected from the network and cannot receive any downlink data. In such a case, the modem can switch to eDRX/DRX mode, then quickly switch to Connected mode.

Table 7: Module Operating Modes

Mode	Description
Active	When the AP is in normal mode and the modem is in connected mode, the module is active and supports all services and functions. The current consumption in active mode is higher than that in sleep modes.
Light Sleep	Generally, when the AP is in idle mode and the modem is not in PSM mode, the module enters Light Sleep mode. In Light Sleep mode, the current consumption of the module is reduced greatly.
Deep Sleep	When the AP is in idle mode and the modem is in PSM, the module enters Deep Sleep mode in which the CPU is powered off and only the 32 kHz RTC clock keeps working. In Deep Sleep mode, the current consumption is minimized (typical value: 800 nA).

3.4. Power Saving

3.4.1. Light Sleep

In Light Sleep mode, the UART serial port does not work, and the module can be woken up on the falling

edge of PSM_EINT or by your sending the command **AT** to it via the main UART port.

3.4.2. Deep Sleep

The module consumes extremely low current in Deep Sleep mode (typical value: 800 nA). The main purpose of Deep Sleep is to reduce the power consumption of the module and prolong the power supply duration of the battery. In this mode, the serial port does not work.

The following figure shows the power consumption of the module in different modes.

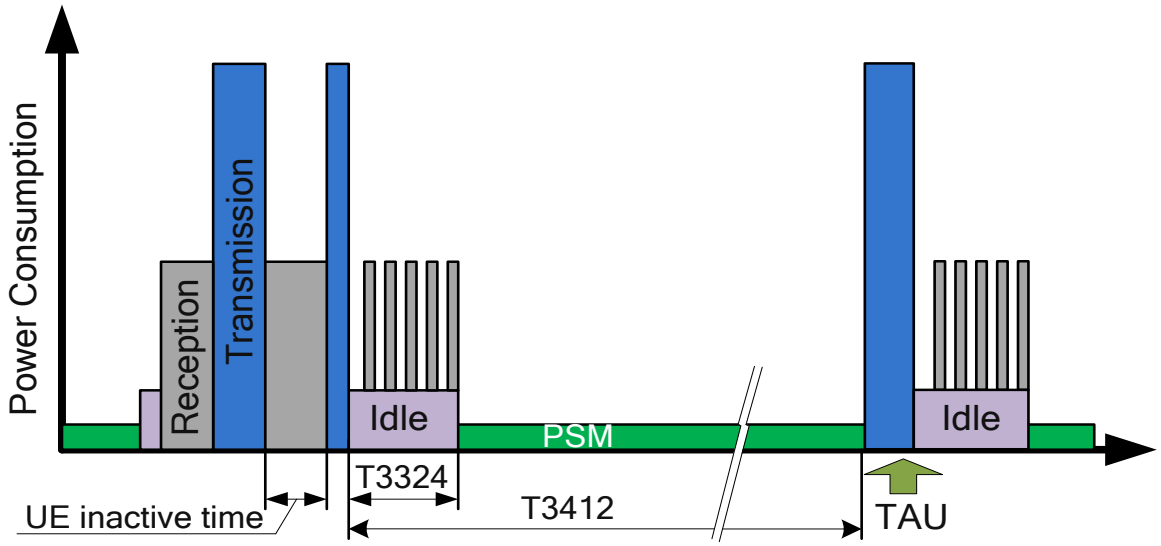


Figure 3: Module Power Consumption in Different Modem Modes

When the modem remains in PSM and the AP is in idle mode, the module will enter Deep Sleep mode. The procedure of the modem entering PSM is as follows:

The modem requests to enable PSM with an **ATTACH REQUEST** or **TAU REQUEST** message during ATTACH or TAU (Tracking Area Update) procedure. Then the network accepts the request and provides an active time value (T3324) to the modem and the mobile reachable timer starts. When the T3324 timer expires, the modem enters PSM. Please note that the module cannot request entering PSM when establishing an emergency attachment or initializing the PDN (Public Data Network) connection

When the module is in Deep Sleep mode, it can be woken up in the following cases:

- After the T3412 timer expires, the module will exit from Deep Sleep automatically.
- Send an AT command to the module (this AT command will be lost), pull down the MAIN_RXD, and in falling edge, the module will be woken up from Deep Sleep.
- Pulling down PSM_EINT (falling edge) will wake up the module from Deep Sleep.

The timing of waking up the module from PSM is illustrated below.

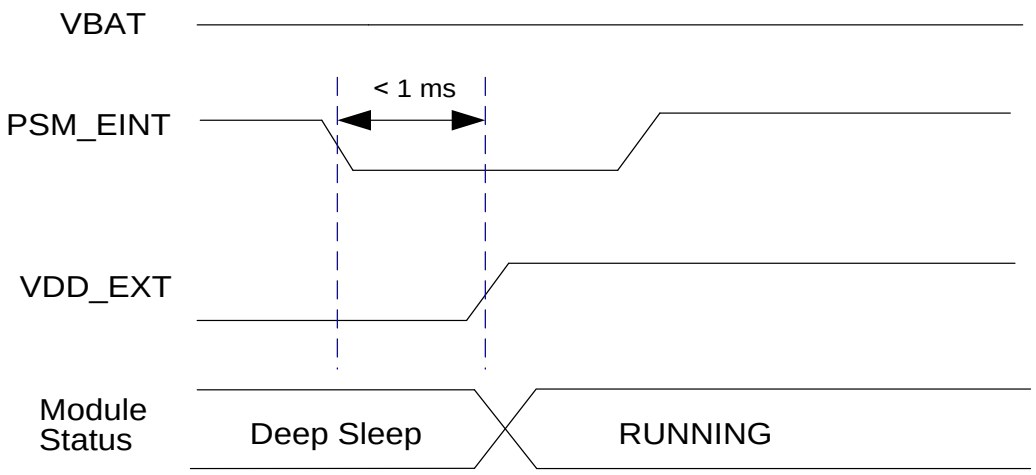


Figure 4: Timing of Waking Up Module from PSM

3.5. Power Supply

3.5.1. Power Supply Pins

The module provides two VBAT pins for connection with an external power supply. The table below describes the module's VBAT and ground pins.

Table 8: Power Supply Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT	42, 43	Power supply for the module	2.2	3.3	4.3	V
GND	1, 27, 34, 36, 37, 40, 41, 56, 57, 58		-	-	-	V

3.5.2. Power Supply Reference Design

Power design for a module is critical to its performance. It is recommended to use a low quiescent current LDO with an output capacity of 0.5 A to regulate the power supply for BC660K-GL. Lithium-thionyl chloride (Li-SOCl2) batteries and Lithium manganese oxide (LiMn2O4) batteries can be used as the power supply. The supply voltage of the module ranges from 2.2 V to 4.3 V. When the module is working, ensure its input voltage never drops below 2.2 V; otherwise, the module cannot work normally.

For better power performance, it is recommended to place a 100 μF tantalum capacitor with low ESR (ESR = 0.7 Ω) and three ceramic capacitors (100 nF, 100 pF and 22 pF) near the VBAT pins. Also, it is recommended to add a TVS diode on the VBAT trace (near VBAT pins) to improve surge voltage

withstanding capability. In principle, the longer the VBAT trace is, the wider it should be. A reference circuit for power supply is illustrated in the following figure.

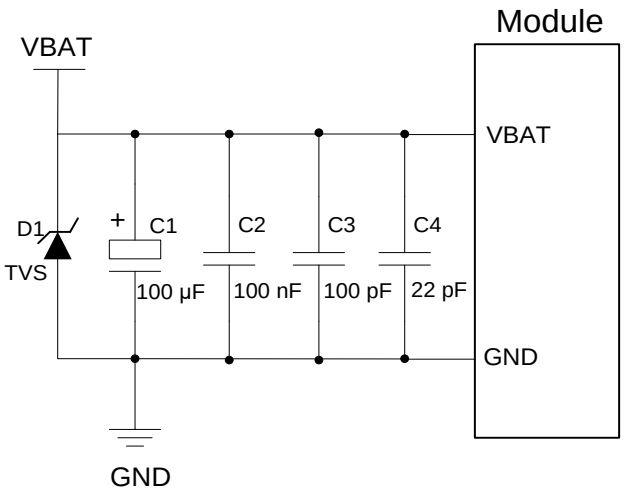


Figure 5: Reference Design for Power Supply

3.5.3. Power Supply Voltage Detection

You can use **AT+CBC** to monitor and query the current VBAT voltage. The unit of the voltage value is mV (millivolt). For detailed information about the command, see ***document [2]***.

3.6. Turn-on/Turn-off Scenario

3.6.1. Turn On

After the module VBAT is powered on, keep the RESET_N and BOOT high (default), and the module will turn on automatically. The turn-on timing is illustrated in the following figure.

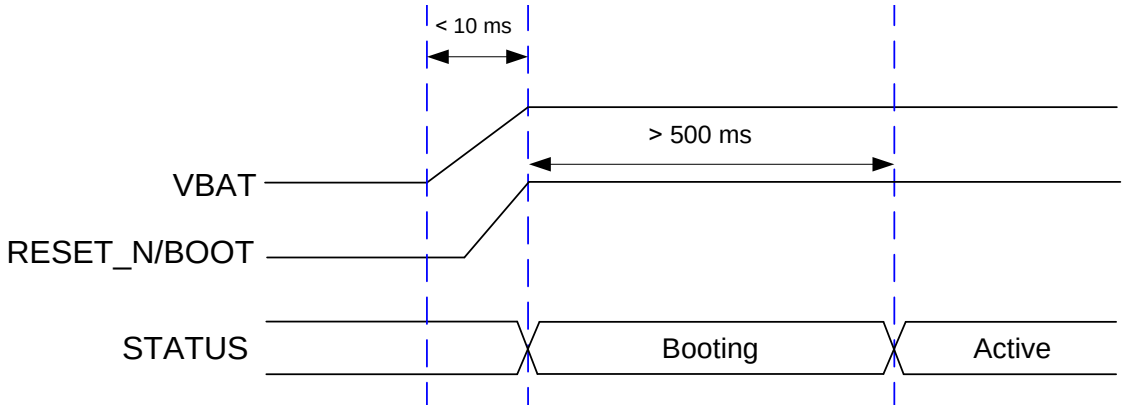


Figure 6: Turn-on Timing

NOTES

1. After the module is powered off, it can be turned on again only after its VBAT voltage drops below 0.7 V. The actual discharging time of VBAT needs to be determined based on circuit tests and enough time margin should be left to avoid abnormal module startup.
2. The power-up time of VBAT must be within 10 ms.
3. It is recommended that the MCU retains a RESET_N controlling pin so that when the abnormal power-on sequence causes the module to boot up abnormally, the RESET_N pin can make the module reset so as to exit from the abnormal state.
4. After VBAT is powered on, RESET_N and BOOT automatically rise to high level due to internal pull-ups.

3.6.2. Turn Off

The module can be turned off through cutting off its VBAT power supply.

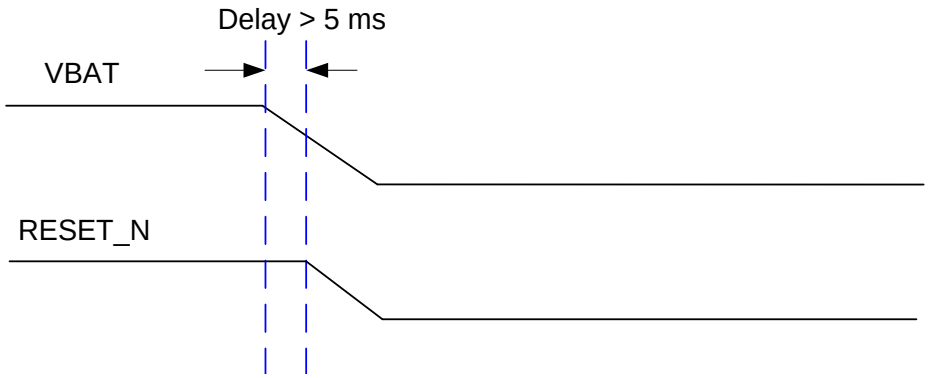


Figure 7: Turn-off Timing

3.6.3. Reset

Driving RESET_N low for at least 50 ms resets the module.

Table 9: Reset Pin Definition

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	15	Reset the module.	V_{IL}max = 0.42 V V_{IH}min = 1.33 V V_{IH}max = 2.2 V	Reset pull-down time ≥ 50 ms Active low.

The reference designs for resetting the module are shown below. An open drain/collector driving circuit or a button can be used to control the RESET_N pin.

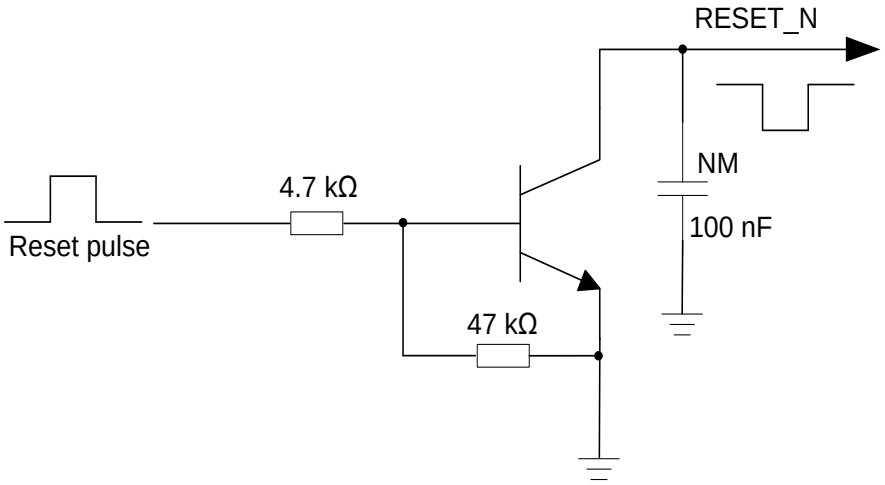


Figure 8: Reference Design for RESET_N Controlled with an OC/OD Driving Circuit

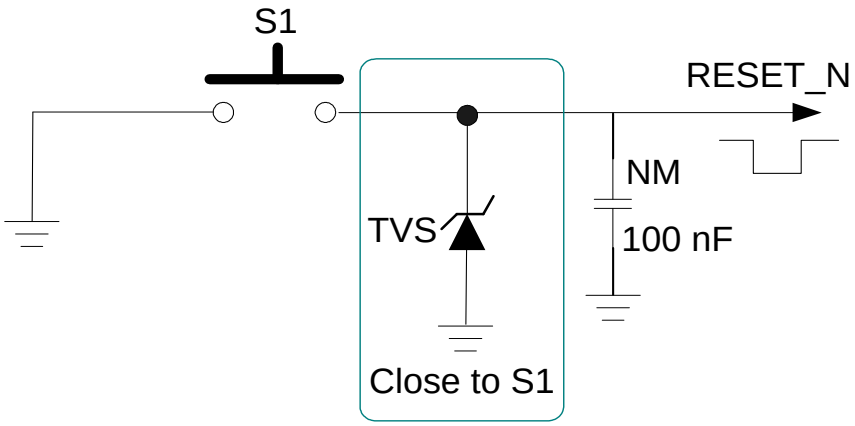


Figure 9: Reference Design for RESET_N Controlled with a Button

NOTE

It is recommended to reserve a 100 nF capacitor position; the capacitor is not mounted by default.

3.6.4. Download Mode

Table 10: Boot Pin Definition

Pin Name	Pin No.	Description	DC Characteristics	Comment
BOOT	7	Make the module enter download mode	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	Active low.

In the process of module reset or powering on, drive and keep the BOOT pin low and the module will enter the download mode.

In the download mode, the firmware can be downloaded through the main serial port. After the download is completed, the module needs to be reset to exit from the download mode.

A reference design is shown below

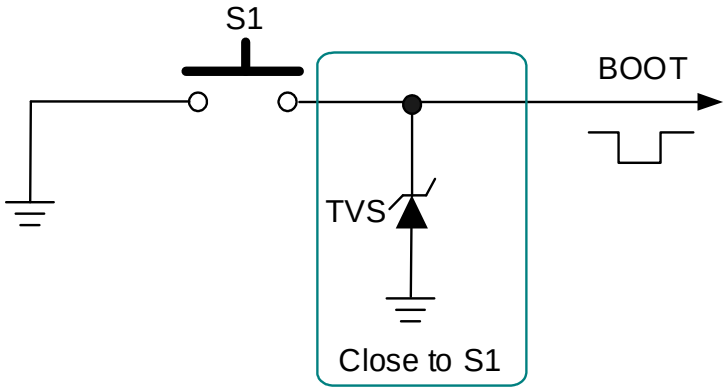


Figure 10: Reference Design for BOOT Controlled with a Button

NOTE

If the BOOT pin is connected to a filter capacitor in parallel, the capacitance of the capacitor cannot be higher than 33 pF.

3.7. UART Interfaces

The module provides two UART ports: the main UART port and the debug UART port. The module is designed as DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection.

Table 11: Pin Definition of UART Interfaces

Interface	Pin Name	Pin No.	Description
Main UART Port	MAIN_TXD	17	Main UART transmit
	MAIN_RXD	18	Main UART receive
Debug UART Port	DBG_RXD	38	Debug UART receive

	DBG_TXD	39	Debug UART transmit
Ring Indication	RI	20	Ring indication (when there is a SMS or a URC output, the module will inform DTE with the RI pin)

3.7.1. Main UART Port

The main UART port supports AT command communication, data transmission and firmware upgrade.

- Default baud rate: 115200 bps
- Supported baud rates: 2400 bps, 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps

When the port is used for firmware upgrade, the baud rate is 921600 bps by default.

When the module is in Deep Sleep/Light Sleep mode, you can wake up it by sending AT commands through the main UART port. It is recommended to keep sending the command **AT** until **OK** is returned before sending AT commands for other services.

The figure below shows the connection between DCE and DTE.

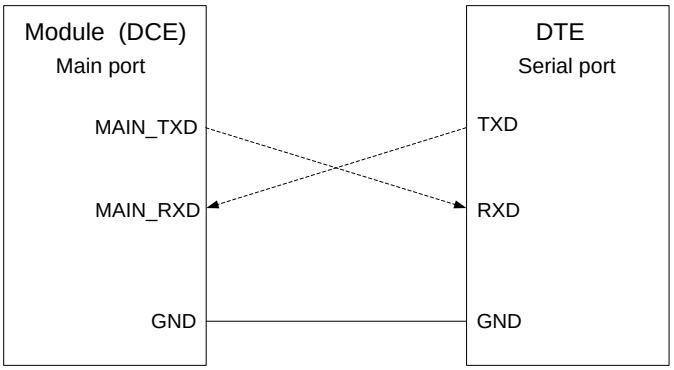


Figure 11: Reference Design for Main UART Port

3.7.2. Debug UART Port

Through debug tools, the debug UART port can be used to output logs for firmware debugging. Its baud rate is 6 Mbps by default. The following is a reference design of debug UART port.

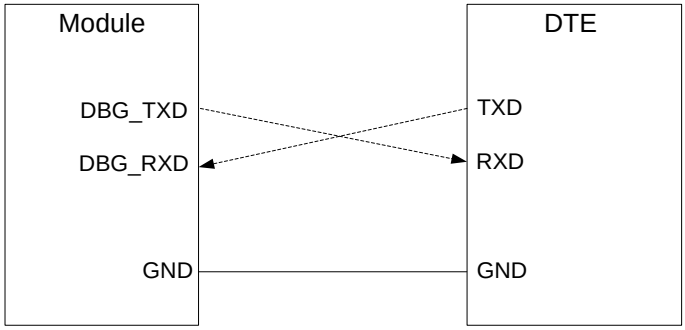


Figure 12: Reference Design for Debug UART Port

3.7.3. UART Application

The serial port voltage domain of this module is optional. Customers can select the appropriate voltage domain through VIO_SEL according to actual situation. When VIO_SEL is floating, the VDD_EXT voltage domain is 1.8 V; when VIO_SEL is grounded, the VDD_EXT voltage domain is 3.3 V or equals the VBAT voltage[1)].

If the voltage domain of your application system is 1.8 V, VIO_SEL can be floating; If the voltage domain of your application system is 3.3 V, VIO_SEL must be grounded.

The following figure shows the reference design of UART:

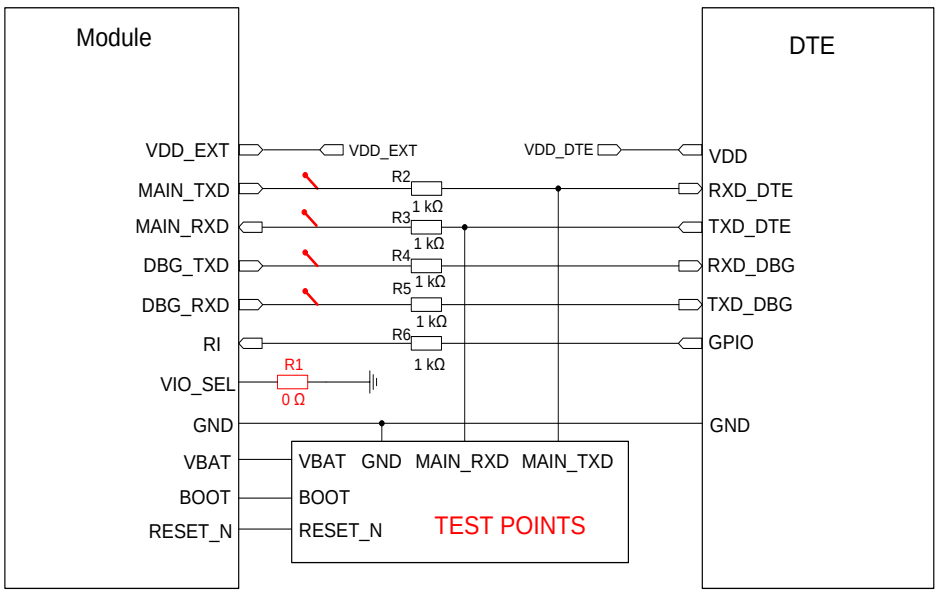


Figure 13: Reference Design for UART

The following circuit shows a reference design for the communication between the module and a PC with a standard RS-232 interface. Make sure to select appropriate voltage domain through VIO_SEL

according to the actual situation.

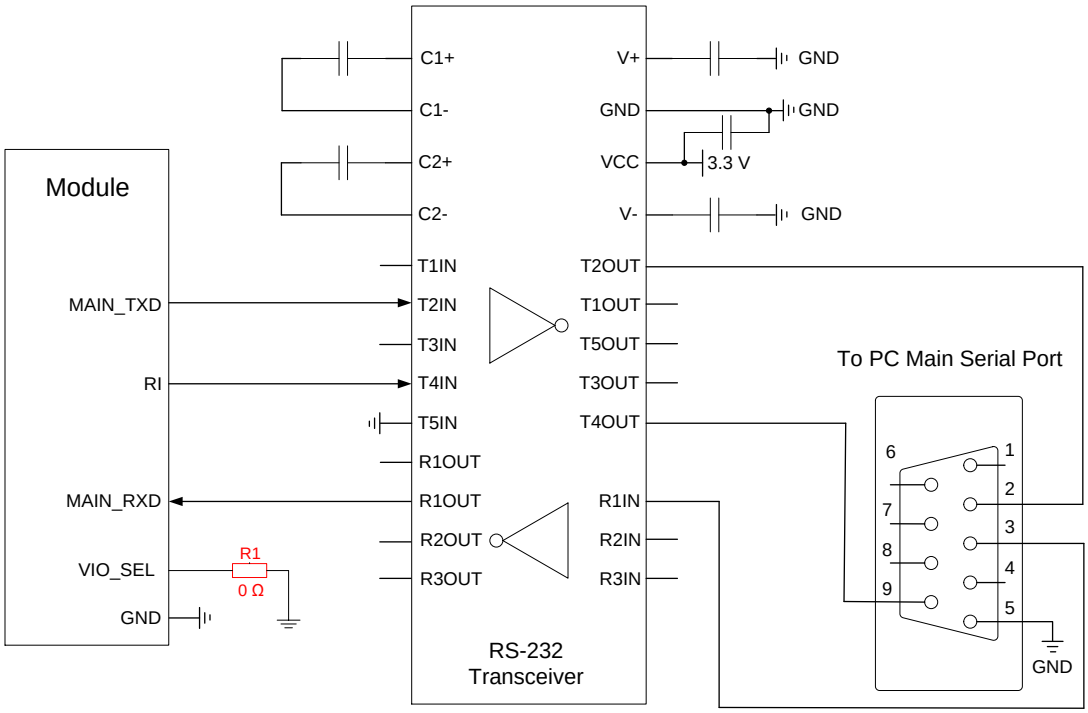


Figure 14: Reference Design for Module-PC Communication via RS-232 Interface

Please visit vendors' websites to select a suitable RS-232 transceiver, such as http://www.exar.com and http://www.maximintegrated.com.

NOTES

1. If the voltage domain of your application system is 1.8 V, keep the R1 in red not mounted; if it is 3.3 V, keep the R1 in red mounted.
2. "" represents the test points of UART interfaces. It is recommended to reserve the test points of VBAT, BOOT and RESET_N for convenient firmware upgrade and debugging when necessary.
3. MAIN_RXD cannot be pulled up to VDD_EXT directly. To pull up MAIN_RXD to VDD_EXT, you need to connect a Schottky diode in series first, and then add a pull-up resistor of 4.7–20 kΩ. For more details, see ***document [3]***.
4. [1)] When VIO_SEL is grounded and VBAT < 3.3 V, VDD_EXT = VBAT;
When VIO_SEL is grounded and VBAT ≥ 3.3 V, VDD_EXT = 3.3 V;
When VIO_SEL is floating, VDD_EXT = 1.8 V.

When the serial port voltage is neither 1.8 V nor 3.3 V, it is recommended to use a level conversion circuit. For the design of the circuit shown in the dotted line, refer to that shown in the solid lines, and pay attention to the connection direction. In this case, the design of RI – GPIO circuit can refer to that of the MAIN_TXD – RXD circuit.

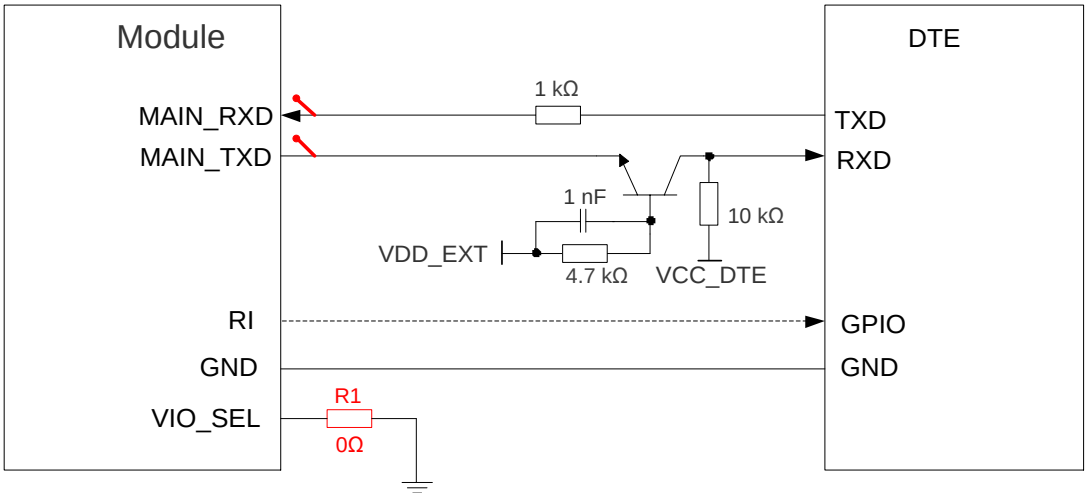


Figure 15: Reference Design for Level Conversion Circuit

NOTES

1. Due to the anti-backflow design of the MAIN_RXD pin, it can be directly connected to the TXD of DTE in 1.8–3.3 V voltage domain. If wake-up function of MAIN_RXD in Deep Sleep/Light Sleep mode is enabled, it is recommended that MAIN_RXD not use any level conversion circuit so as to avoid abnormal wake-up.
2. If you apply the level conversion circuit, don't mount the R1 marked in red.
3. MAIN_RXD cannot be pulled up to VDD_EXT directly. To pull up MAIN_RXD to VDD_EXT, you need to connect a Schottky diode in series first, and then add a pull-up resistor of 4.7–20 kΩ. For more details, see ***document [3]***.
4. The level conversion circuit does not apply to applications with high baud rates exceeding 460 kbps.

3.8. USIM Interface

The USIM card is powered by USIM_VDD. Both 1.8 V and 3.0 V USIM cards are supported.

Table 12: Pin Definition of USIM Interface

Pin Name	Pin No.	Description	Comment
USIM_VDD	14	USIM card power supply	When 3.0 V ≤ VBAT ≤ 4.3 V, support 1.8/3.0 V USIM card; When 2.2 V ≤ VBAT < 3 V, only support 1.8 V USIM card;

		Maximum supply current: about 80 mA.
USIM_CLK	13	USIM card clock
USIM_RST	12	USIM card reset
USIM_DATA	11	USIM card data
USIM_GND	10	Dedicated ground for USIM card

A reference design for the USIM interface with a 6-pin USIM card connector is below.

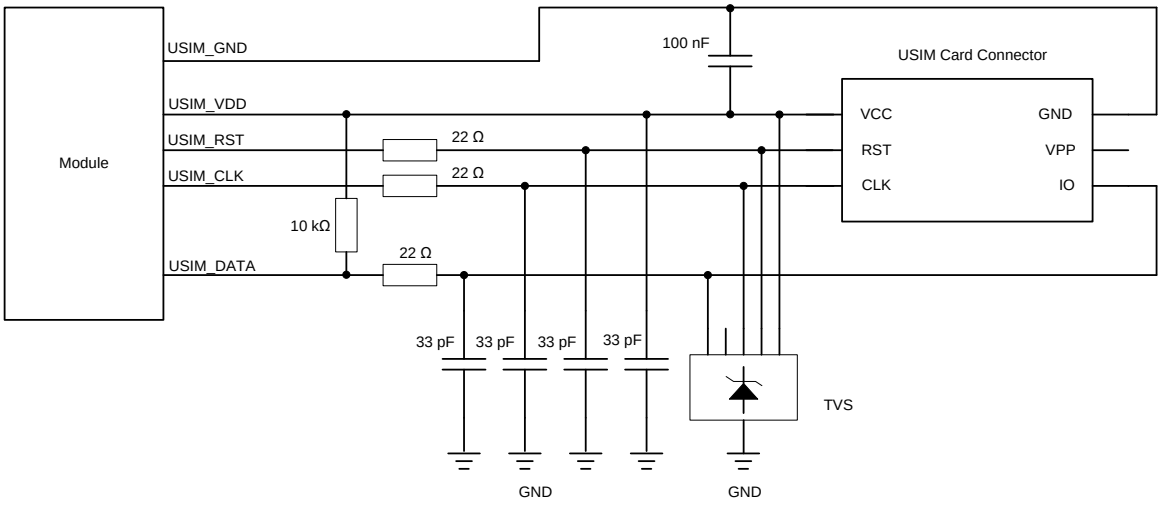


Figure 16: Reference Design for USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the criteria below in USIM circuit design:

- Place the USIM card connector as close to the module as possible and keep the trace length as less than 200 mm as possible.
- Keep USIM card signal lines away from RF and VBAT traces.
- Make the trace between the ground of the module and that of the USIM card connector short and wide and ensure the trace width no less than 0.5 mm avoid any decrease in electric potential. The decoupling capacitor between USIM_VDD and GND should be not more than 1 μF and be placed close to the USIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them separately with surrounding ground.
- To offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should be not more than 50 pF. Place the ESD protection device as close to the USIM card connector as possible, and ensure the USIM card signal lines from the USIM card connector go through the ESD protection device before reaching the module. The 22 Ω resistors should be

connected in series between the module and the USIM card connector to suppress EMI spurious transmission and enhance ESD protection. Note that the module's USIM peripheral devices should be placed close to the USIM card connector.

NOTE

The pull-up resistor of 10 kΩ on the USIM_DATA line can improve anti-jamming capability and should be placed close to the USIM card connector.

3.9. ADC Interface

The module provides a 12-bit ADC input channel to read the voltage value.

Table 13: Pin Definition of ADC Interface

Pin Name	Pin No.	Description	Comment
ADC0	9	Analog to digital converter interface	Voltage range: 0–1.2 V

NOTE

A 320 kΩ pull-down resistor is integrated inside the ADC pin. This resistor needs to be considered when you calculate the voltage division relationship.

3.10. RI Interface

When there is a message received or a URC output, the module will notify DTE through the RI interface.

Table 14: Pin Definition of RI Interface

Pin Name	Pin No.	Description	Comment
RI	20	Ring indication	VDD_EXT power domain

Table 15: RI Signal Status

Module Status	RI Signal Level
Standby	High
URC/Message Arrives	Low for at least 120 ms before starting data output.

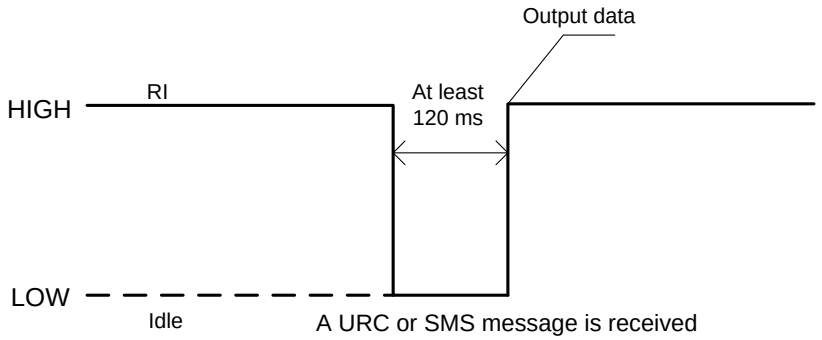


Figure 17: RI Behaviour When a URC/Message is Received

3.11. GPIO Interfaces

The module provides four general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** command can be used to configure the status of the GPIO pins. For more details about the AT command, see ***document [2]***.

Table 16: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	Description
GPIO1	3	General-purpose input/output
GPIO2	4	General-purpose input/output
GPIO3	5	General-purpose input/output
GPIO4	6	General-purpose input/output

3.12. GRFC Interfaces*

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 17: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	Description	Comment
GRFC1	54	Generic RF controller	1.8 V power domain. If unused, keep these pins open.
GRFC2	55	Generic RF controller	

3.13. NETLIGHT Interface*

NETLIGHT can be used to indicate the network status of the module.

Table 18: Pin Definition of NETLIGHT Interface

Pin Name	Pin No.	Description	Comment
NETLIGHT	16	Indicate the module's network activity status	-

A reference design for NETLIGHT is shown below.

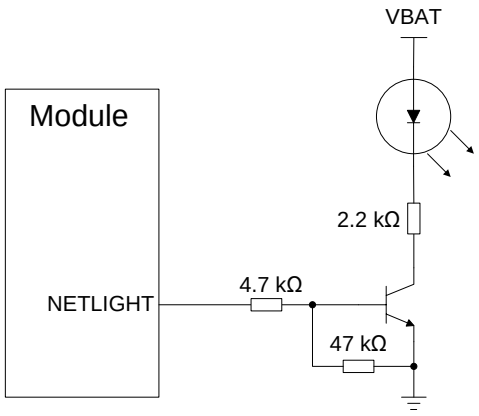


Figure 18: Reference Design for NETLIGHT

NOTE

"*" means under development.

4 Antenna Interface

The pin 35 is the RF antenna pad. The antenna port has an impedance of 50 Ω.

4.1. Pin Definition

Table 19: Pin Definition of NB-IoT Antenna Interface

Pin Name	Pin No.	Description
ANT_RF	35	RF antenna interface
GND	34, 36, 37	Ground

4.2. Operating Frequency

Table 20: Module Operating Frequency

Frequency Band	Receiving Frequency	Transmitting Frequency
B1	2110–2170 MHz	1920–1980 MHz
B2	1930–1990 MHz	1850–1910 MHz
B3	1805–1880 MHz	1710–1785 MHz
B4	2110–2155 MHz	1710–1755 MHz
B5	869–894 MHz	824–849 MHz
B8	925–960 MHz	880–915 MHz
B12	729–746 MHz	699–716 MHz
B13	746–756 MHz	777–787 MHz

B14	758–768 MHz	788–798 MHz
B17	734–746 MHz	704–716 MHz
B18	860–875 MHz	815–830 MHz
B19	875–890 MHz	830–845 MHz
B20	791–821 MHz	832–862 MHz
B25	1930–1995 MHz	1850–1915 MHz
B28	758–803 MHz	703–748 MHz
B66	2110–2180 MHz	1710–1780 MHz
B70	1995–2020 MHz	1695–1710 MHz
B85	728–746 MHz	698–716 MHz

4.3. RF Antenna Reference Design

BC660K-GL provides an RF antenna pin for external NB-IoT antenna connection.

- The RF trace on the host PCB should be a coplanar waveguide or microstrip whose characteristic impedance is 50 Ω.
- The module comes with ground pads which are next to the antenna pad to give a better grounding.
- To achieve better RF performance, it is recommended to reserve a π type matching circuit and place the π-type matching components (R1/C1/C2) as close to the antenna as possible. By default, the capacitors (C1/C2) are not mounted and a 0 Ω resistor is mounted on R1.

A reference design of the RF interface is shown below.

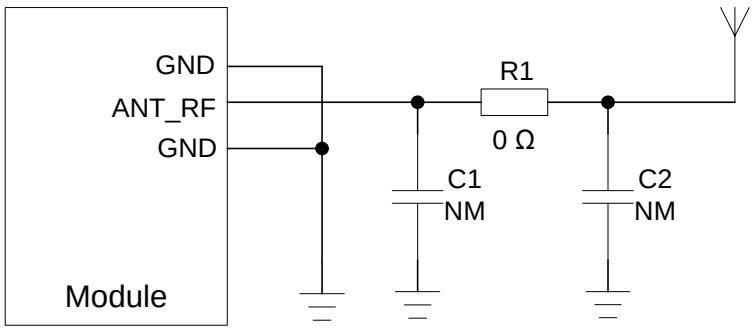


Figure 19: Reference Design for NB-IoT Antenna Interface

4.4. Reference Design of RF Layout

The characteristic impedance of all RF traces on your PCB should be controlled at 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the material's dielectric constant, the height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). The microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs for microstrip or coplanar waveguide transmission lines with different PCB structures.

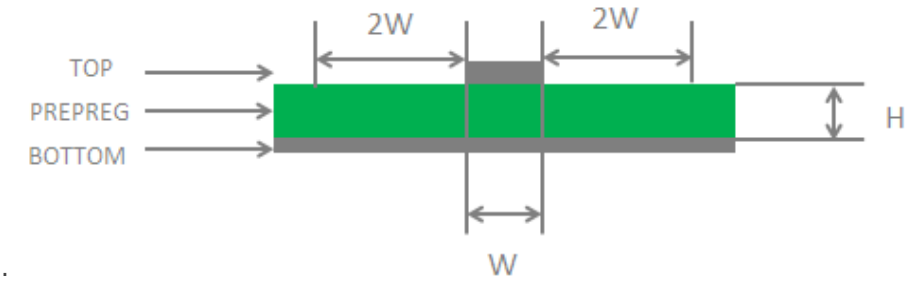


Figure 20: Microstrip on a 2-layer PCB

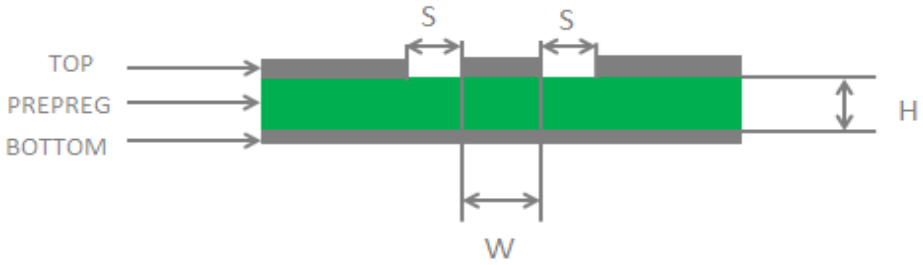


Figure 21: Coplanar Waveguide on a 2-layer PCB

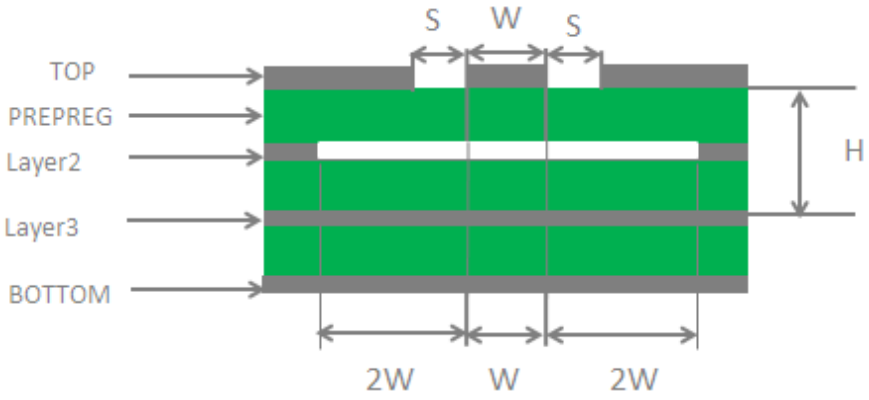


Figure 22: Coplanar Waveguide on a 4-layer PCB (Layer 3 as Reference Ground)

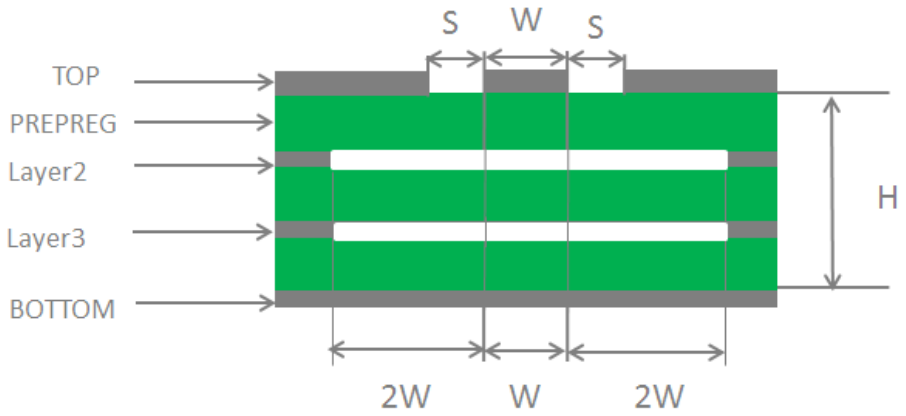


Figure 23: Coplanar Waveguide on a 4-layer PCB (Bottom Layer as Reference Ground)

To ensure reliable RF performance, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces at 50 Ω.
- The GND pins adjacent to the RF pin should not be designed as thermal relief pads, and should be fully grounded.
- The distance between the RF pin and the RF connector should be as short as possible, and all the right-angle traces should be changed to curve ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground helps to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2 × W).

For more details on the reference design of RF Layout, see ***document [4]***.

4.5. Antenna Requirements

To minimize the loss on RF trace and RF cable, pay attention to the antenna design. The following tables show the requirements on an NB-IoT antenna.

Table 21: Antenna Cable Insertion Loss Requirements

Band	Requirements
LTE B5/B8/B12/B13/B14/B17/B18/B19/B20/B28/B85	Cable insertion loss: < 1 dB
LTE B1/B2/B3/B4/B25/B66/B70	Cable insertion loss: < 1.5 dB

Table 22: Required Antenna Parameters

Parameters	Requirements
Frequency Range	698–2200 MHz
VSWR	≤ 2
Efficiency	> 30 %
Max Input Power (W)	50
Input Impedance (Ω)	50

4.6. RF Output Power

Table 23: RF Conducted Output Power

Frequency Band	Max.	Min.
B1	23 dBm ±2 dB	< -39 dBm
B2	23 dBm ±2 dB	< -39 dBm
B3	23 dBm ±2 dB	< -39 dBm
B4	23 dBm ±2 dB	< -39 dBm
B5	23 dBm ±2 dB	< -39 dBm
B8	23 dBm ±2 dB	< -39 dBm
B12	23 dBm ±2 dB	< -39 dBm
B13	23 dBm ±2 dB	< -39 dBm
B14	23 dBm ±2 dB	< -39 dBm
B17	23 dBm ±2 dB	< -39 dBm
B18	23 dBm ±2 dB	< -39 dBm
B19	23 dBm ±2 dB	< -39 dBm
B20	23 dBm ±2 dB	< -39 dBm

B25	23 dBm ±2 dB	< -39 dBm
B28	23 dBm ±2 dB	< -39 dBm
B66	23 dBm ±2 dB	< -39 dBm
B70	23 dBm ±2 dB	< -39 dBm
B85	23 dBm ±2 dB	< -39 dBm

NOTE

The design conforms to the NB-IoT radio protocols in *3GPP Rel.13*.

4.7. RF Receiving Sensitivity

Table 24: RF Receiving Sensitivity

Frequency Band	With RF Retransmission	Without RF Retransmission
B1	≤ -129 dBm	-116 dBm
B2	≤ -129 dBm	-116 dBm
B3	≤ -129 dBm	-116 dBm
B4	≤ -129 dBm	-116 dBm
B5	≤ -129 dBm	-116 dBm
B8	≤ -129 dBm	-116 dBm
B12	≤ -129 dBm	-116 dBm
B13	≤ -129 dBm	-116 dBm
B14	≤ -129 dBm	-116 dBm
B17	≤ -129 dBm	-116 dBm
B18	≤ -129 dBm	-116 dBm
B19	≤ -129 dBm	-116 dBm

B20	≤ -129 dBm	-116 dBm
B25	≤ -129 dBm	-116 dBm
B28	≤ -129 dBm	-116 dBm
B66	≤ -129 dBm	-116 dBm
B70	≤ -129 dBm	-116 dBm
B85	≤ -129 dBm	-116 dBm

4.8. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose Electric.

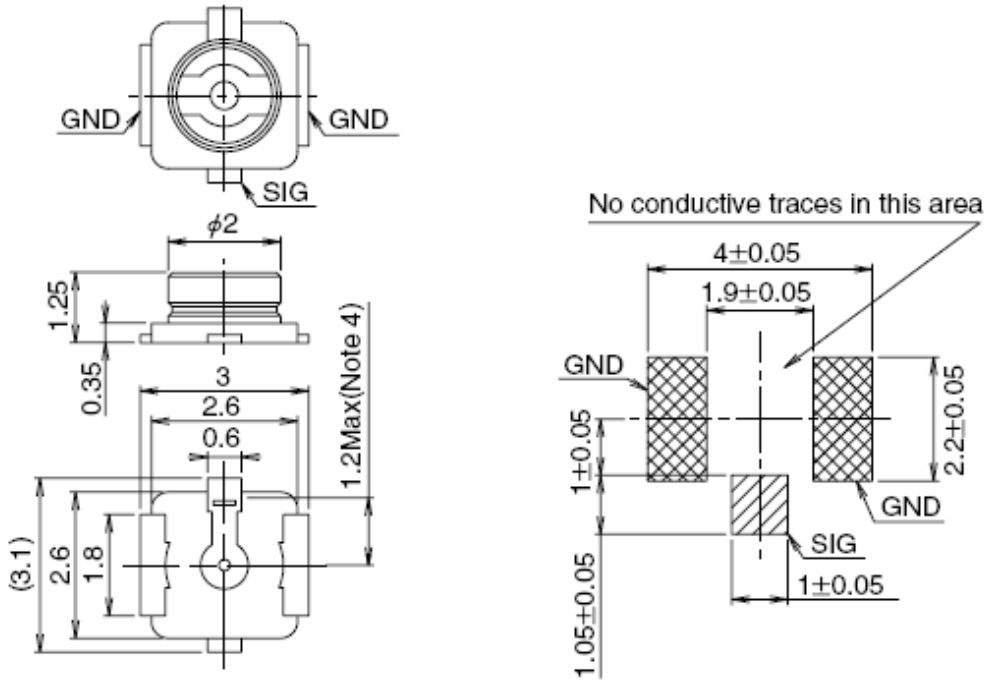


Figure 24: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

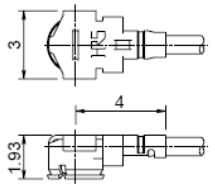
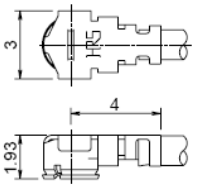
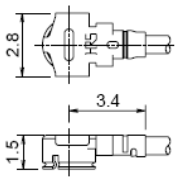
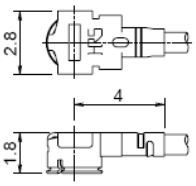
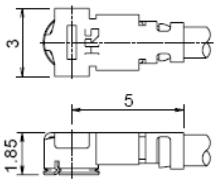
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 25: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connectors.

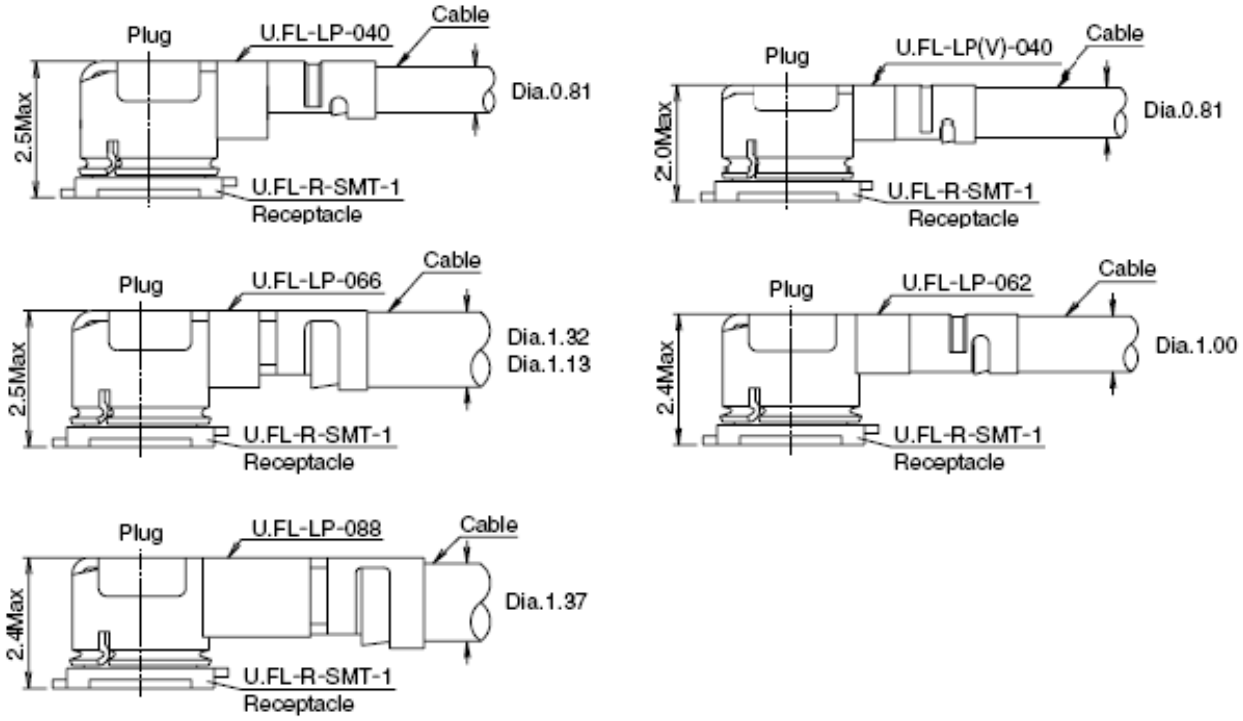


Figure 26: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

5 Reliability and Electrical Characteristics

5.1. Operating and Storage Temperatures

The following table lists the operating and storage temperatures of the module.

Table 25: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module maintains functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

5.2. Current Consumption

The table below lists the current consumption of BC660K-GL under different states.

Table 26: Module Current Consumption (3.3 V VBAT Power Supply)

Deep Sleep						
AP Mode	**Modem Mode**		**Min.**	**Typ.**	**Max.**	**Unit**
Idle	PSM		-	0.8	-	μA
Light Sleep						
AP Mode	**Modem Mode**		**Min.**	**Typ.**	**Max.**	**Unit**
Idle	eDRX = 40.96 s, PTW = 10.24 s, ECL = 0		-	38	-	μA
	@ DRX = 1.28 s		-	220	-	μA
	@ DRX = 2.56 s		-	110	-	μA
Active [1]						
AP Mode	**Modem Mode**		**Min.**	**Typ.**	**Max.** [2]	**Unit**
Normal	Single-tone (15 kHz subcarrier spacing)	B1 @ 23.4dBm	-	111	300	mA
		B2 @ 22.5 dBm	-	108	305	mA
		B3 @ 22.5 dBm	-	100	280	mA
		B4 @ 22.5 dBm	-	100	277	mA
		B5 @ 23.2 dBm	-	98	270	mA
		B8 @ 23.1 dBm	-	105	299	mA
		B12 @ 23.3 dBm	-	120	332	mA
		B13 @ 23.2 dBm	-	100	283	mA
		B14 @ 23.3 dBm	-	100	282	mA
		B17 @ 23.2 dBm	-	115	325	mA
		B18 @ 23.2 dBm	-	94	265	mA
		B19 @ 23.2 dBm	-	95	270	mA
		B20 @ 23.2 dBm	-	98	272	mA
		B25 @ 22.5 dBm	-	108	301	mA

	B28 @ 23.3 dBm	-	109	310	mA
	B66 @ 22.5 dBm	-	101	280	mA
	B70 @ 22.6 dBm	-	104	276	mA
	B85 @ 23.2 dBm	-	115	329	mA
Single-tone (3.75 kHz subcarrier spacing)	B1 @ 23.2 dBm	-	240	311	mA
	B2 @ 22.7 dBm	-	230	296	mA
	B3 @ 22.8 dBm	-	213	274	mA
	B4 @ 23 dBm	-	212	273	mA
	B5 @ 22.9 dBm	-	202	263	mA
	B8 @ 22.8 dBm	-	221	298	mA
	B12 @ 23.1 dBm	-	259	328	mA
	B13 @ 22.8 dBm	-	218	279	mA
	B14 @ 22.8 dBm	-	217	278	mA
	B17 @ 23.1 dBm	-	252	325	mA
	B18 @ 23.1 dBm	-	199	258	mA
	B19 @ 22.9 dBm	-	201	260	mA
	B20 @ 22.9 dBm	-	207	267	mA
	B25 @ 22.7 dBm	-	232	297	mA
	B28 @ 23.1 dBm	-	240	306	mA
	B66 @ 22.8 dBm	-	213	274	mA
	B70 @ 22.7 dBm	-	216	273	mA
	B85 @ 23 dBm	-	252	323	mA

NOTES

1. [1)] Power consumption under laboratory instrument test condition.
2. [2)] The “maximum value” in “Active” mode refers to the maximum pulse current during RF emission.

5.3. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics.

Table 27: Electrostatic Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna interface	±5	±10	kV
Other interfaces	±0.5	±1	kV

6 Mechanical Features

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

6.1. Mechanical Dimensions

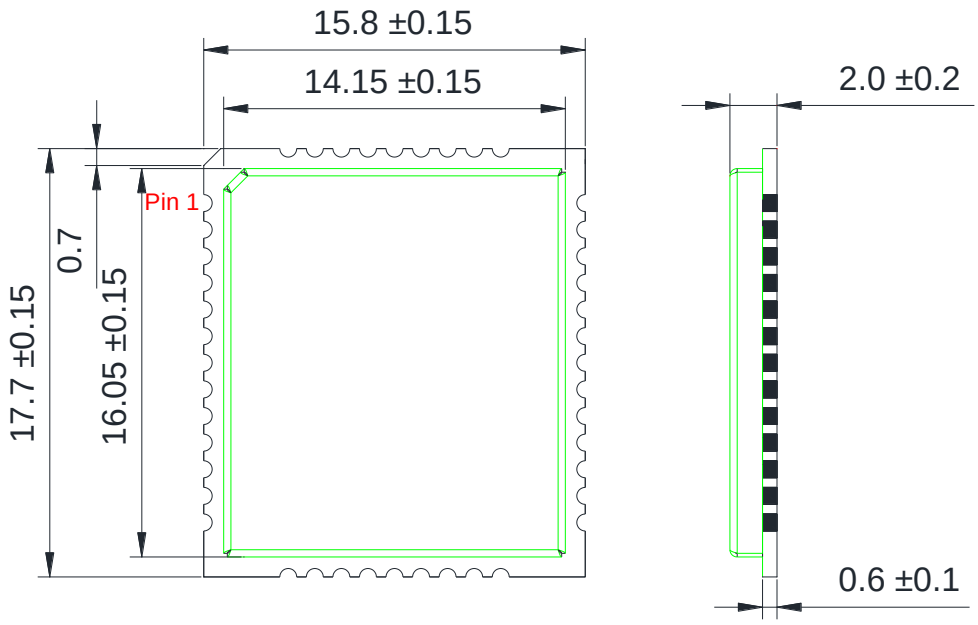


Figure 27: Top and Side Dimensions (Unit: mm)

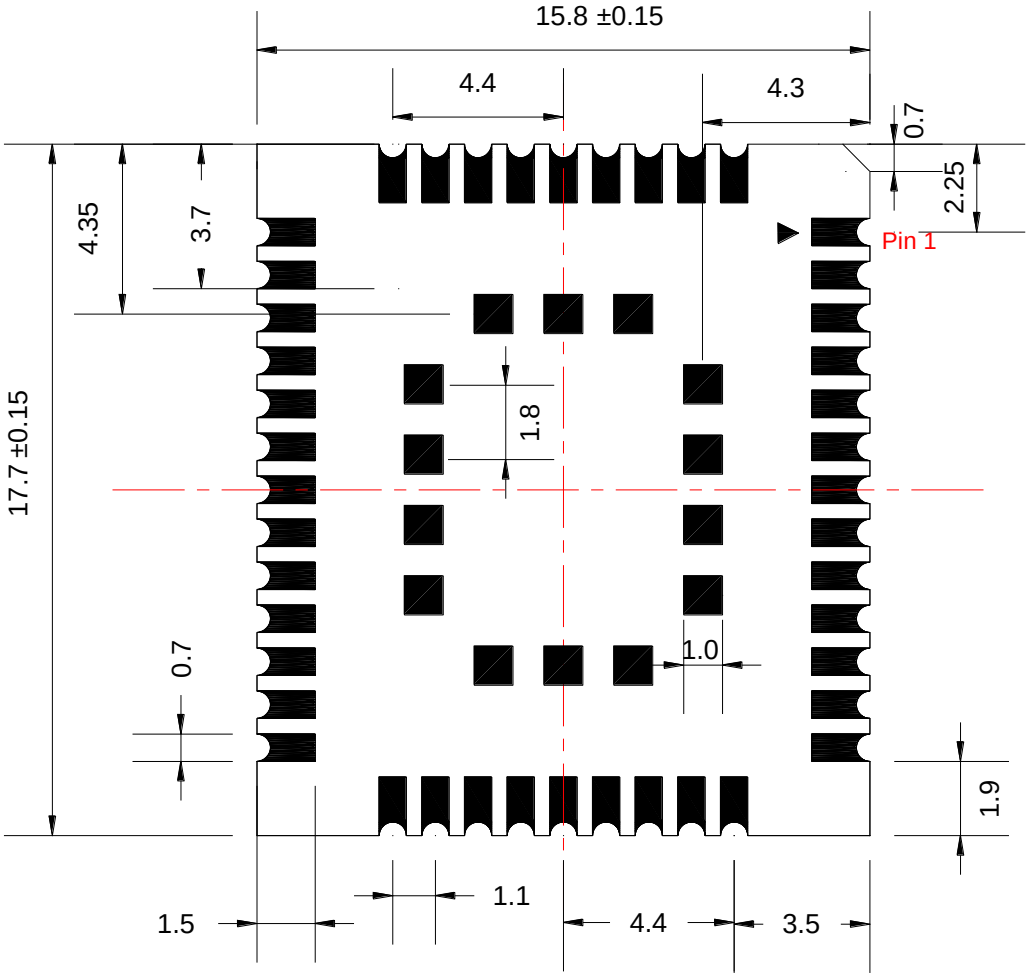


Figure 28: Bottom Dimension (Bottom View)

NOTE

The package warpage level of the module conforms to JEITA ED-7306 standard.

6.2. Recommended Footprint

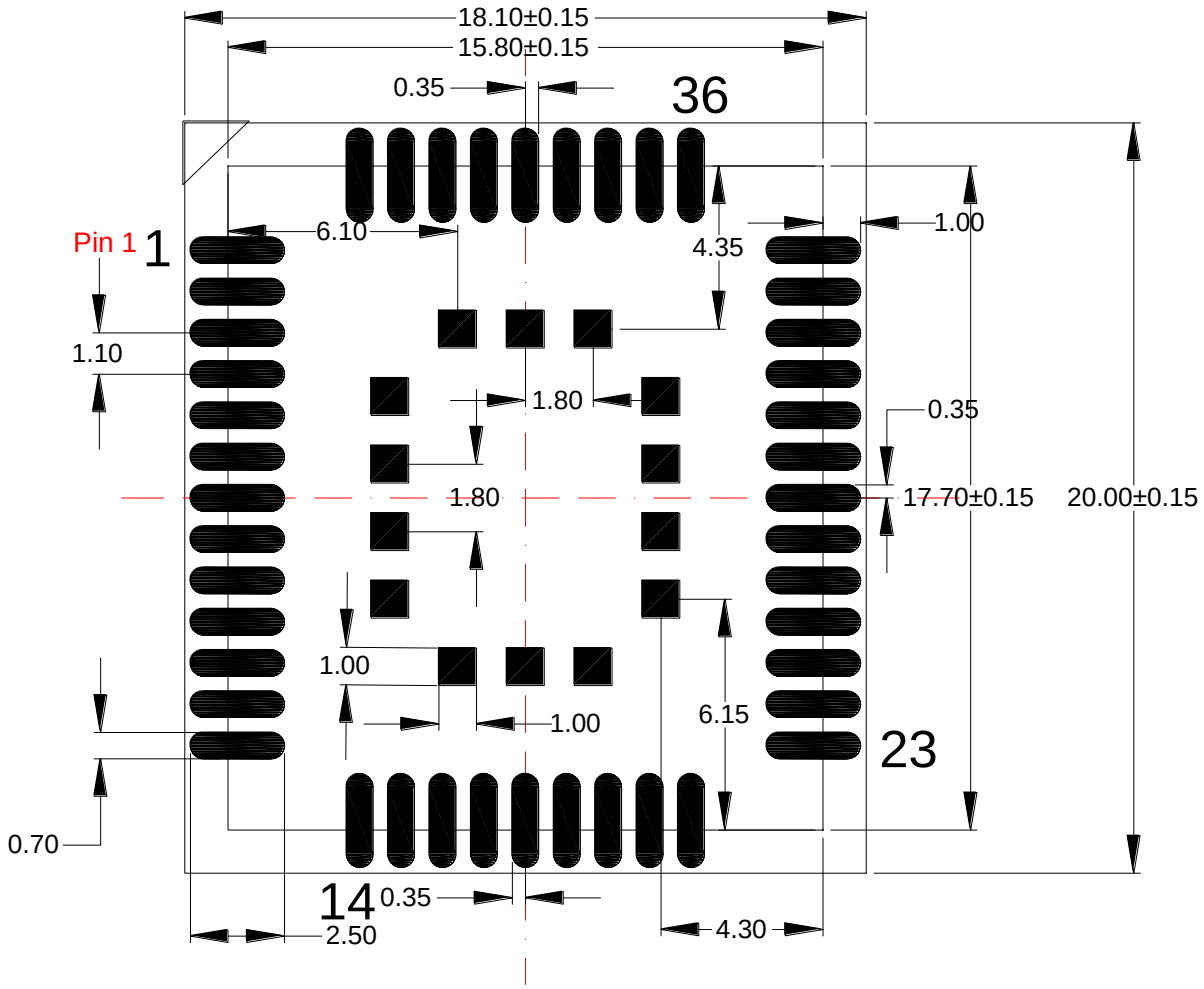


Figure 29: Recommended Footprint (Unit: mm)

NOTE

For easy maintenance of the module, it is recommended to keep about 3 mm between the module and other components on the motherboard.

6.3. Top and Bottom Views

Figure 30: Top View of the Module

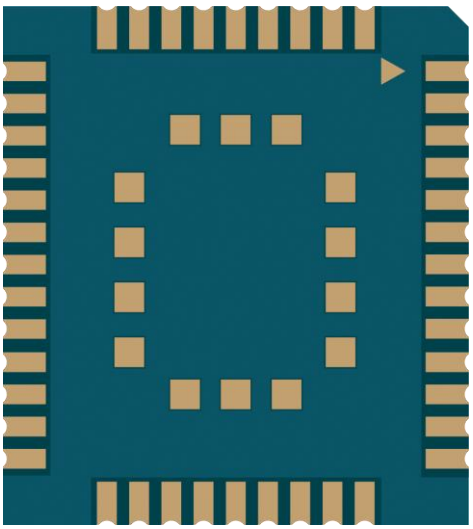


Figure 31: Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Take the module out of the packaging and put it on high-temperature resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [5]***.

It is suggested that the peak reflow temperature is 238 °C to 246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

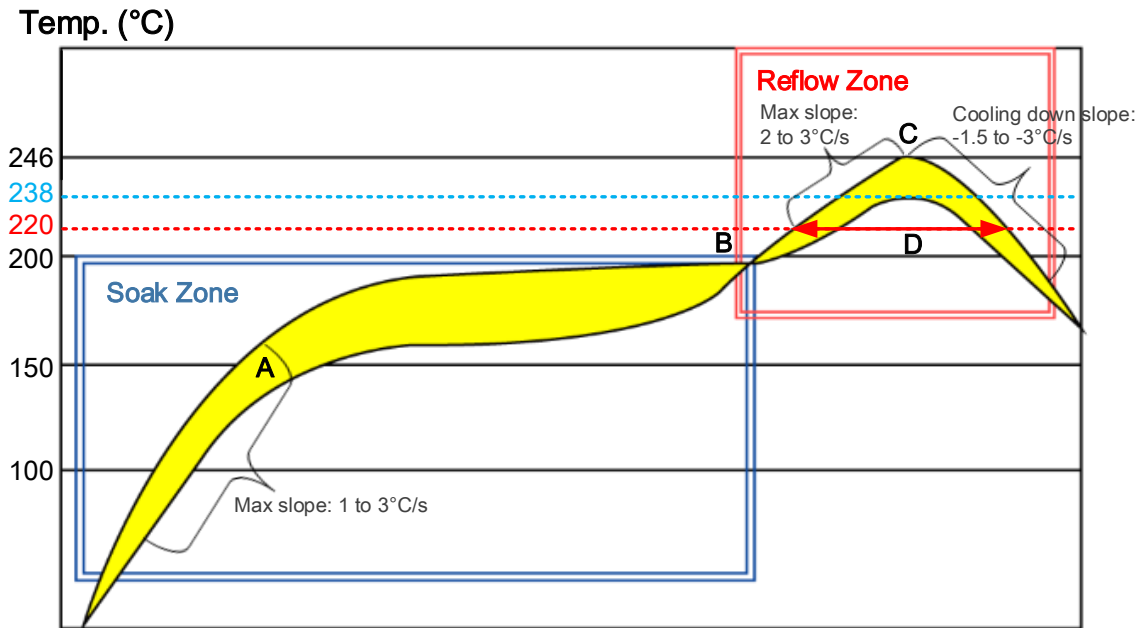


Figure 32: Recommended Reflow Soldering Thermal Profile

Table 28: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220 °C)	45–70 s
Max temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module

7.3. Tape and Reel Packaging

The modules are stored in a vacuum-sealed bag which is ESD-proof. The bag should not be opened until the modules are ready to be soldered onto the application.

The reel is 330 mm in diameter and each reel contains 250 modules.

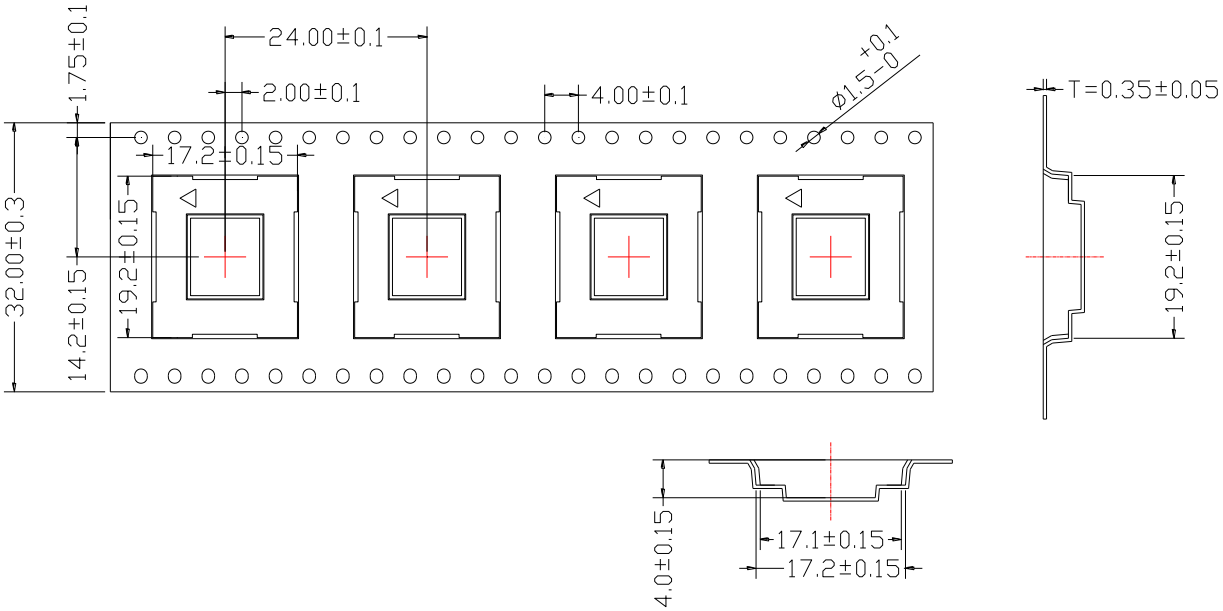


Figure 33: Tape Dimensions (Unit: mm)

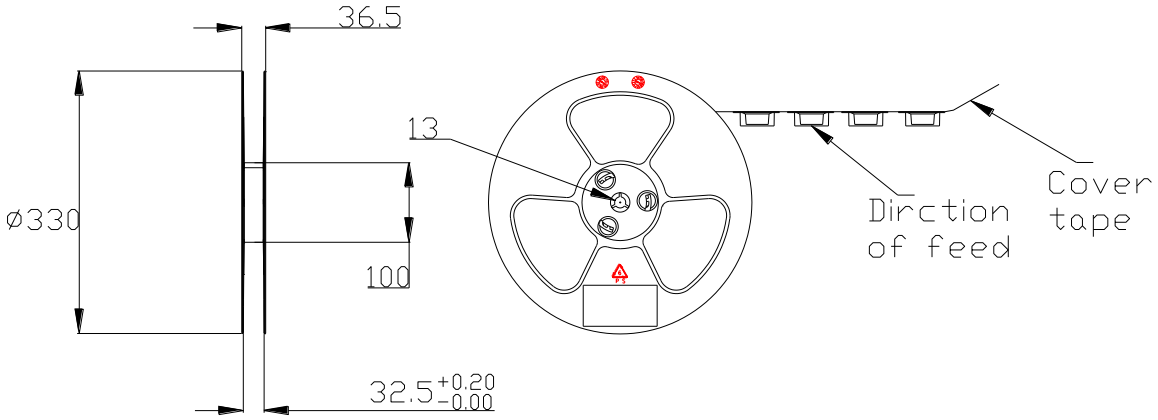


Figure 34: Reel Dimensions (Unit: mm)

8 Appendix References

Table 29: Related Documents

SN	Document Name	Description
[1]	Quectel_BC660K-GL-TE-B_User_Guide	BC660K-GL-TE-B User Guide
[2]	Quectel_BC660K-GL_AT_Commands_Manual	BC660K-GL AT Commands Manual
[3]	Quectel_BC660K-GL_Reference_Design	BC660K-GL Reference Design
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

Table 30: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AP	Application Processor
DCE	Data Communications Equipment
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
DTLS	Datagram Transport Layer Security
eDRX	extended Discontinuous Reception
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
H-FDD	Half Frequency Division Duplexing

HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
I/O	Input/Output
kbps	Kilo Bits Per Second
LED	Light Emitting Diode
LTE	Long Term Evolution
LwM2M	Lightweight M2M
MQTT	Message Queuing Telemetry Transport
NB-IoT	Narrow Band- Internet of Things
OC	Open Collector
OD	Open Drain
PCB	Printed Circuit Board
PDN	Public Data Network
PDU	Protocol Data Unit
PSM	Power Save Mode
PTW	Paging Time Window
RF	Radio Frequency
RTC	Real Time Clock
RXD	Receive Data
SMD	Surface Mount Device
SMS	Short Message Service
TAU	Tracking Area Update
TCP	Transmission Control Protocol
TE	Terminal Equipment
TLS	Transport Layer Security

TXD	Transmitting Data
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	Universal Subscriber Identification Module
VSWR	Voltage Standing Wave Ratio
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$nom	Absolute Noimal Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value