EG065K Series

Hardware Design

LTE-A Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for your failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-03-19	David WANG/ Alex WANG	Creation of the document
1.0	2023-09-01	Iyukee Shen/ Miles LI/ Jacen HUANG	First official release

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1 Introduction

This document defines the EG065K series module and describes its air interfaces and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

This document is applicable to the following modules:

- EG065K-NA
- EG065K-EA

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, and so on, it indicates that the function, feature, interface, pin, AT command, or argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is a SMD type module which is engineered to meet the demanding requirements in M2M applications, such as body camera, portable device, etc. Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

Category	
Packaging and pins number	LGA; 230
Dimensions	(28.0 ±0.2) mm × (31.0 ± 0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 5.3 g
Wireless network functions	LTE/WCDMA*
Variants	EG065K-NA, EG065K-EA

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	EG065K-NA	EG065K-EA
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/ B25/B26/B30/B66	B1/B2/B3/B4/B5/B7/B8/B20/B28
LTE-TDD	-	B40
WCDMA*	-	B1/B2/B3/B4/B5/B8

2.2. Key Features

Table 4: Key Features

Feature	Details
Power Supply	● Supply voltage: 3.3-4.5 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode. ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	● Supports (U)SIM card: 1.8/3.0 V ● Supports Dual SIM Single Standby
PCM Interface*	● Used for audio function with external codec or SLIC ● Supports 16-bit linear data format ● Supports long and short frame synchronization ● Supports master and slave modes, but must be the master mode in long frame synchronization
USB Interface	● Complies with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, firmware upgrade, GNSS NMEA sentence output, software debugging and voice over USB* ● Supports USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x
UART Interfaces	**Main UART interface:** ● Used for AT command communication and data transmission ● Baud rate reaches up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART interface:** ● Used for Linux console and log output ● 115200 bps baud rate
SPI*	● Works as master mode only ● Max. clock frequency rate: 50 MHz
I2C Interface*	● One I2C interface ● Complies with I2C Specification, Version 3.0
I2S Interface*	● Supports 16-bit linear data format ● I2S is a common 4-wire DAI (MCLK is not used in the design normally), used in Hi-Fi, STB and portable devices ● The Tx and Rx lines are used for audio transmission, whilst the bit clock and left/right clock synchronize the link ● I2S in either controller or codec state is able to drive (master) the bit

	clock and left/right clock lines
PCIe Interface	● Complies with *PCI Express Base Specification Revision 2.0* ● Supports 5 Gbps per lane ● Used for data transmission ● RC mode only
Network Indication	Provides NET_MODE and NET_STATUS to indicate network connectivity status
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Quectel enhanced AT commands
Rx-diversity	LTE
Antenna Interface	● 2 main antennas: ANT_MAIN1/ANT_MAIN2 ● 2 diversity antennas: ANT_DRX1/ANT_DRX2 ● 50 Ω impedance 50 Ω impedance
Transmitting Power	● LTE-FDD B30: Class 3 (22.3 dBm ±2 dB) ● LTE-FDD Other bands: Class3 (23.5 dBm ±2 dB) ● LTE-TDD: Class 3 (23.5 dBm ±2 dB) ● WCDMA: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP Rel-12 Cat 6 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports modulations: Uplink: QPSK, 16QAM and 64QAM modulations Downlink: QPSK, 16QAM and 64QAM modulations ● Max. transmission data rates: – LTE-FDD: 300 Mbps (DL)/75 Mbps (UL) – LTE-TDD: 250 Mbps (DL)/45 Mbps (UL) [1]
UMTS* Features	● Supports 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Supports modulations: Uplink: QPSK modulation Downlink: QPSK, 16QAM and 64QAM modulations ● Max. transmission data rates: – DC-HSDPA: 42 Mbps (DL) – WCDMA: 384 kbps (DL)/384 kbps (UL) [1]
Internet Protocol Features	Supports QMI/MBIM/NITZ/HTTP/HTTPS/FTP/LwM2M/PING

[1] LTE-TDD is only supported by EG065K-EA.

Temperature Ranges	● Operating temperature range [2]: -30 °C to 75 °C ● Extended temperature range [3]: -40 °C to 85 °C ● Storage temperature range: -40 °C to 90 °C
Firmware Upgrade	● USB interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[2] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[3] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this extended temperature range, the module remains the ability to establish and maintain functions such as voice*, SMS, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are impervious, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR2 SDRAM + NAND Flash
- Radio frequency
- Peripheral interface

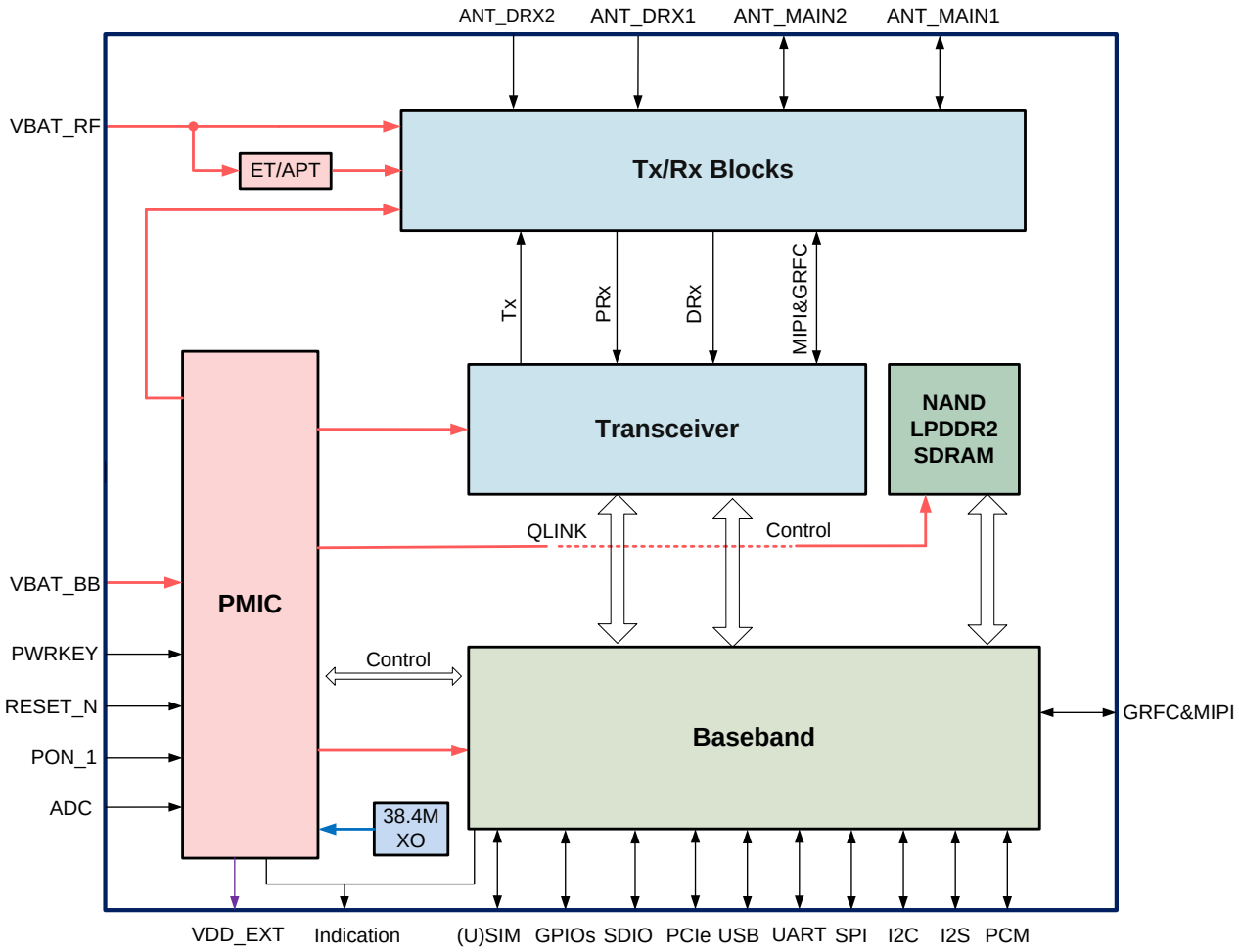


Figure 1: Functional Diagram

2.4. Pin Assignment

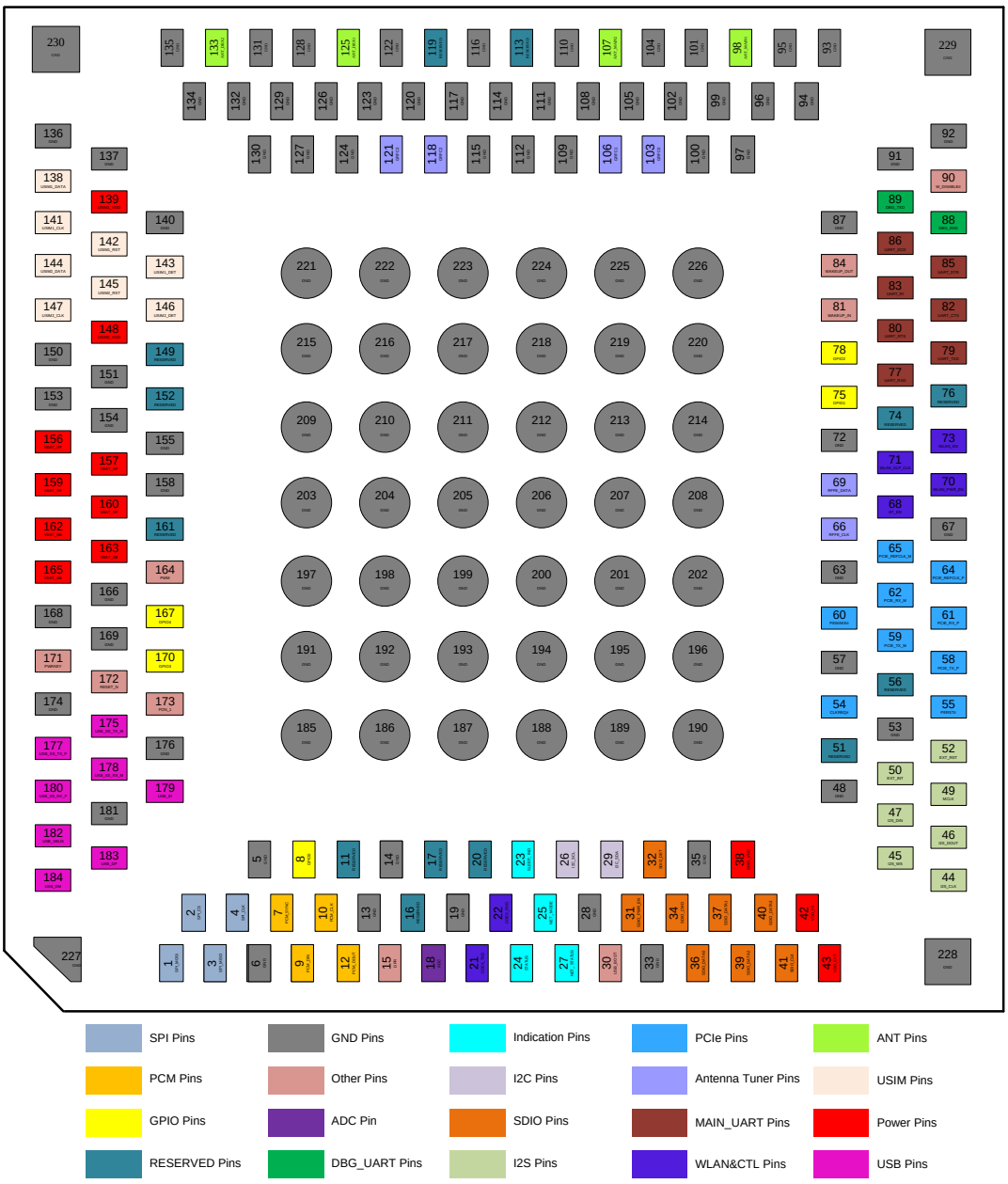


Figure 2: Pin Assignment (Top View)

NOTE

Keep all RESERVED pins unconnected.

2.5. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output
PD	Pull Down

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	162, 163, 165.	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	156, 157, 159, 160	PI	Power supply for the module's RF part	Vmax = 4.5 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.2 A in a transmitting burst.
VDD_EXT	43	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	A test point is recommended to be reserved.
VDD_P2	42	PI	SD card IO power supply	For high-voltage: Vmax = 3.05 V	If SD Card is used，connect VDD_P2 to SDIO_VDD.

				Vnom = 2.85 V Vmin = 2.7 V For low-voltage: Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	If eMMC is used or nothing on SDIO interface, connect VDD_P2 to VDD_EXT.
GND	5,6,13,14,19,28,33,35,48,53,57,63,67,72,87,91,92,93,94,95,96,97,99,100,101,102, 104,105,108,109,110,111,112,114,115,116,117,120,122,123,124,126,127,128,129, 130,131,132,134,135,136,137,140,150,151,153,154,155,158,166,168,169,174,176, 181,185–230				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	171	DI	Turn on/off the module	1.8 V	Internally pulled up to 1.8 V. Active low. A test point is recommended to be reserved if unused.
RESET_N	172	DI	Reset the module		
PON_1	173	DI	Turns on the module automatically when it is pulled high	V_{IH}max = VBAT+0.5 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Pull it up to 1.8–4.5 V. If unused, pull it down to GND.
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	24	DO	Indicate the module's operation status	1.8 V	If unused, keep them open.
NET_MODE	25	DO	Indicate the module's network registration mode		
NET_STATUS	27	DO	Indicate the module's network activity status		
SLEEP_IND	23	DO	Indicate the module's sleep mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	182	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.3 V Vnom = 5.0 V	For USB connection detection only, not power supply. A test point must be reserved.
USB_ID*	179	DI	USB ID detect	1.8 V	

USB_DP	183	AIO	USB differential data (+)		Comply with USB 2.0 specifications. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	184	AIO	USB differential data (-)		
USB_SS_TX_M	175	AO	USB 3.0 super-speed transmit (-)		Comply with USB 3.0 specifications. Require differential impedance of 90 Ω.
USB_SS_TX_P	177	AO	USB 3.0 super-speed transmit (+)		
USB_SS_RX_P	180	AI	USB 3.0 super-speed receive (+)		
USB_SS_RX_M	178	AI	USB 3.0 super-speed receive (-)		
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	64	AO	PCIe reference clock (+)		Require differential impedance of 95 Ω. If unused, keep them open.
PCIE_REFCLK_M	65	AO	PCIe reference clock (-)		
PCIE_TX_P	58	AO	PCIe transmit (+)		
PCIE_TX_M	59	AO	PCIe transmit (-)		
PCIE_RX_P	61	AI	PCIe receive (+)		
PCIE_RX_M	62	AI	PCIe receive (-)		
CLKREQ#	54	DI	PCIe clock request	1.8 V	It is an input signal. If unused, keep it open.
PERST#	55	DO	PCIe RC reset		It is an output signal. If unused, keep it open.
PEWAKE#	60	DI	PCIe wake up		It is an input signal. If unused, keep it open.
SDIO Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_VDD	38	PO	**SD card application**: SDIO pull up power source **eMMC application**: Keep it open as used for eMMC	1.8/3.0 V	The module supports either 1.8 V or 3.0 V automatically. Cannot work as SD card power supply. SD card must be powered by an external power supply.

SDIO_PWR_EN	31	DO	SDIO power enable	1.8 V	If unused, keep them open.
SDIO_DET	32	DI	SD card detect		
SDIO_CMD	34	DIO	SDIO command	SDIO_VDD	If unused, keep them open.
SDIO_CLK	41	DO	SDIO clock		
SDIO_DATA0	36	DIO	SDIO data bit 0		
SDIO_DATA1	37	DIO	SDIO data bit 1		
SDIO_DATA2	39	DIO	SDIO data bit 2		
SDIO_DATA3	40	DIO	SDIO data bit 3		
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	139	PO	(U)SIM1 card power supply	USIM1_VDD 1.8/3.0 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	138	DIO	(U)SIM1 card data		
USIM1_CLK	141	DO	(U)SIM1 card clock		
USIM1_RST	142	DO	(U)SIM1 card reset		
USIM1_DET	143	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_VDD	148	PO	(U)SIM2 card power supply	USIM2_VDD 1.8/3.0V	If USIM2 interface is unused, keep it open.
USIM2_DATA	144	DIO	(U)SIM2 card data		If USIM2 interface is unused, keep it open.
USIM2_CLK	147	DO	(U)SIM2 card clock		If USIM2 interface is unused, keep it open.
USIM2_RST	145	DO	(U)SIM2 card reset		If USIM2 interface is unused, keep it open.
USIM2_DET	146	DI	(U)SIM2 card hot-plug detect	1.8 V	If USIM2 interface is unused, keep it open.

MAIN UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	77	DI	Main UART receive	1.8 V	If unused, keep them open.
MAIN_TXD	79	DO	Main UART transmit		
MAIN_RTS	80	DI	Request to send signal to the module		RTS: Connect to the MCU's RTS.
MAIN_CTS	82	DO	Clear to send signal from the module		CTS: Connect to the MCU's CTS.
MAIN_DCD	86	DO	Main UART data carrier detect		If unused, keep them open.
MAIN_RI	83	DO	Main UART ring indication		
MAIN_DTR	85	DI	Main UART data terminal ready		Pulled up by default. Pulling low will awaken the module. If unused, keep it open. Sleep mode control
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	88	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	89	DO	Debug UART transmit		
SPI*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_MOSI	1	DO	SPI master-out slave-in	1.8 V	If unused, keep them open. Master mode only.
SPI_CLK	4	DO	SPI clock		
SPI_MISO	3	DI	SPI master-in slave-out		
SPI_CS	2	DO	SPI chip select		
I2C Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SDA	29	OD	I2C serial data (for external codec)	1.8 V	Pull each of them up to VDD_EXT with an external 4.7 kΩ resistor. If unused, keep them open.
I2C_SCL	26	OD	I2C serial clock (for external codec)		

PCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	7	DIO	PCM data frame sync	1.8 V	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_DIN	9	DI	PCM data input		If unused, keep it open.
PCM_CLK	10	DIO	PCM clock		In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_DOUT	12	DO	PCM data output		If unused, keep it open.
I2S Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_WS	45	DIO	I2S word select	1.8 V	If unused, keep them open.
I2S_SCK	44	DIO	I2S clock		
I2S_DIN	47	DI	I2S data in		
I2S_DOUT	46	DO	I2S data out		
MCLK	49	DO	Clock output for codec		
EXT_RST	52	DO	External audio reset		
EXT_INT	50	DI	External audio interrupt		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO0	8	DIO	General-purpose input/output	1.8 V	
GPIO1	75	DIO	General-purpose input/output		
GPIO2	78	DIO	General-purpose input/output		
GPIO3	170	DIO	General-purpose input/output		
GPIO4	167	DIO	General-purpose input/output		

RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN1	98	AIO	Main antenna interface LTE LMB_TRX ● For EG065K-NA, LMB includes B2/B4/B5/B12/B13/ B14/B25/B26/B66 ● For EG065K-EA, LMB includes B1/B2/B3/B4/B5/B8 /B20/B28 WCDMA LMB_TRX ● For EG065K-NA, LMB includes B2/B4/B5 ● For EG065K-EA, LMB includes B1/B2/B3/B4/B5/B8		50 Ω impedance.
ANT_MAIN2	107	AIO	Main antenna interface LTE HB_TRX ● For EG065K-NA, HB includes B7/B30 ● For EG065K-EA, HB includes B7/B40		
ANT_DRX1	125	AI	Diversity antenna interface LTE MHB_DRX ● For EG065K-NA, MHB includes B2/B4/B7/B25/B30/ B66 ● For EG065K-EA, MHB includes B1/B2/B3/B4/B7/ B40 WCDMA MB_DRX ● For EG065K-NA, MB includes B2/B4 ● For EG065K-EA,		

			MB includes B1/B2/B3/B4		
ANT_DRX2	133	AI	Diversity antenna interface LTE LB_DRX ● For EG065K-NA, LB includes B5/B12/B13/B14/B26 ● For EG065K-EA, LB includes B5/B8/B20/B28 WCDMA LB_DRX ● For EG065K-NA, LB includes B5 ● For EG065K-EA, LB includes B5/B8		
RFFE Antenna Tuner Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RFFE_CLK	66	DO	Used for external MIPI IC control	1.8 V	If unused, keep them open.
RFFE_DATA	69	DIO	Used for external MIPI IC control		
GRFC Generic RF controller					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC0	103	DO	Generic RF controller	1.8 V	If unused, keep them open.
GRFC1	106	DO			
GRFC2	118	DO			
GRFC3	121	DO			
WLAN Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_ PWR_EN	70	DO	WLAN power supply enable control	1.8 V	If unused, keep them open.
COEX_TXD	21	DO	LTE/WLAN coexistence transmit		

COEX_RXD	22	DI	LTE/WLAN coexistence receive		
WLAN_EN	73	DO	WLAN function enable control		Active high. If unused, keep it open.
WLAN_SLP_CLK	71	DO	WLAN sleep clock		If unused, keep it open.
BT_EN	68	DO	Bluetooth function enable control		If unused, keep it open.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	18	AI	General-purpose ADC interface	Voltage range: 0 to 1.875 V	If unused, keep it open.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	30	DI	Force the module into emergency download mode	1.8 V	Active high. A test point is recommended to be reserved.
W_DISABLE#	90	DI	Airplane mode control		Pulled up by default. At low voltage level, the module will enter airplane mode. If unused, keep it open.
DPR	15	DI	Dynamic power reduction		Active low.
WAKEUP_IN	81	DI	Wake up the module		Pulled up by default. Low level wakes up the module. If unused, keep it open.
WAKEUP_OUT	84	DO	Wake up the host		Pulled down by default. High level wakes up the host. If unused, keep it open.
PWM	164	DO	PWM output		
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	11,16,17,20,51,56,74,76,113,119,149,152,161				Keep them unconnected.

2.6. EVB Kit

Quectel supplies an evaluation board (UMTS and LTE EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network and ready to send and receive data.
	Voice*/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** sets the module to a minimum functionality mode. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or driving W_DISABLE# low can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	The current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call* and TCP/UDP data from the network normally.	
Power Down Mode	The power management unit shuts down the power supply. Software goes inactive. All application interfaces are inaccessible. Operating voltage (connected to VBAT_BB and VBAT_RF) remains applied.	

See more details about **AT+CFUN=0** and **AT+CFUN=4** in ***document [2].***

3.2. Sleep Mode

DRX of the module can reduce the power consumption to an ultra-low level during sleep mode. The diagram below illustrates the relationship between the DRX run time and the power consumption of the module in this mode.

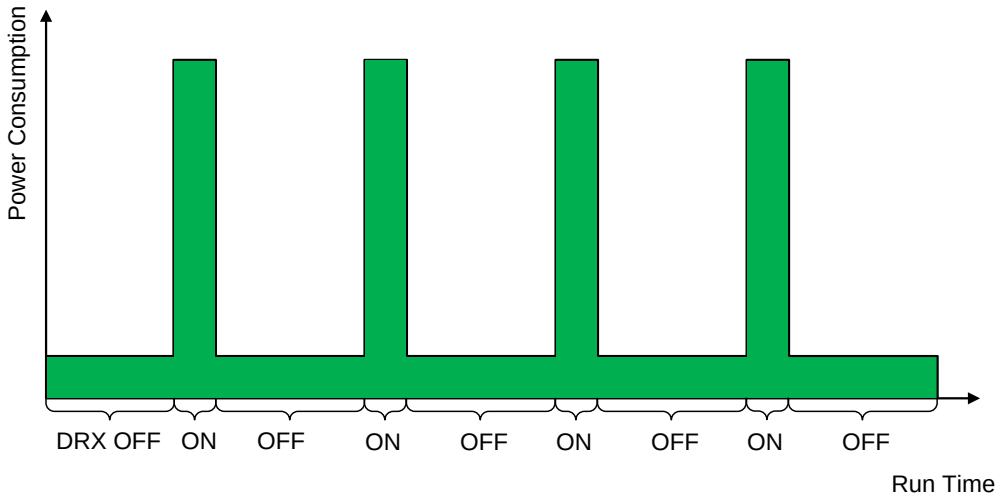


Figure 3: DRX Run Time and Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. USB Application Scenario

For the two situations below, two preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1**.
- The host's USB bus, which connects to the module's USB interface, enters suspend state.

See details of **AT+QSCLK=1** in ***document [2].***

3.2.1.1. USB Application with USB Remote Wakeup Function

The host supports USB suspend/resume and remote wakeup function. The figure below illustrates the connection between the module and the host.

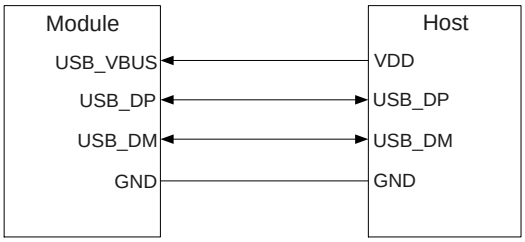


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will be woken up in the following conditions:

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals to host's USB bus to wake up the host.

3.2.1.2. USB Application Without USB Suspend Function

Besides, for this situation below, two preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1**. See details of **AT+QSCLK=1** in ***document [2].***
- Disconnect USB_VBUS.

If the host does not support USB suspend function, USB_VBUS should be disconnected through an external control circuit to set the module enter sleep mode. Turn on the power switch and supply power to USB_VBUS will wake up the module. The figure illustrates the connection between the module and the host.

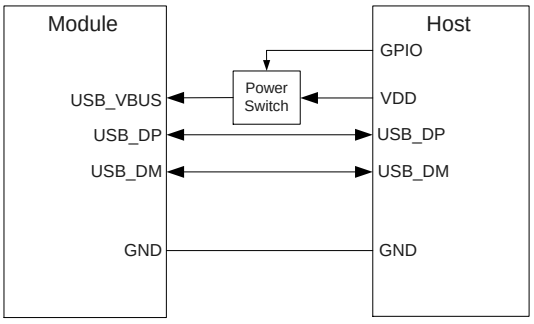


Figure 5: Sleep Mode Application without Suspend Function

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via hardware and software methods, see ***Chapter 4.13*** for details.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 7 VBAT pins dedicated for the connection with the external power supply. There are 2 separate voltage domains for VBAT.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	162, 163, 165	PI	Power supply for the module's baseband part	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	156, 157, 159, 160	PI	Power supply for the module's RF part	It must be provided with sufficient current up to 1.2 A in a transmitting burst.
VDD_EXT	43	PO	Provide 1.8 V for external circuit	A test point is recommended to be reserved.
VDD_P2	42	PI	SD card IO power supply	If SD Card is used, connect VDD_P2 to SDIO_VDD. If eMMC is used or nothing on SDIO interface, connect VDD_P2 to VDD_EXT.
GND	5, 6, 13, 14, 19, 28, 33, 35, 48, 53, 57, 63, 67, 72, 87, 91–97, 99–102, 104, 105, 108–112, 114–117, 120, 122–124, 126–132, 134–137, 140, 150, 151–155, 158, 166, 168, 169, 174, 176, 181, 185–230			

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power supply design. The continuous current of the power supply should be 2.0 A at least and the peak current should be 3.0 A at least.

The following figure shows a reference design for +5.0 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

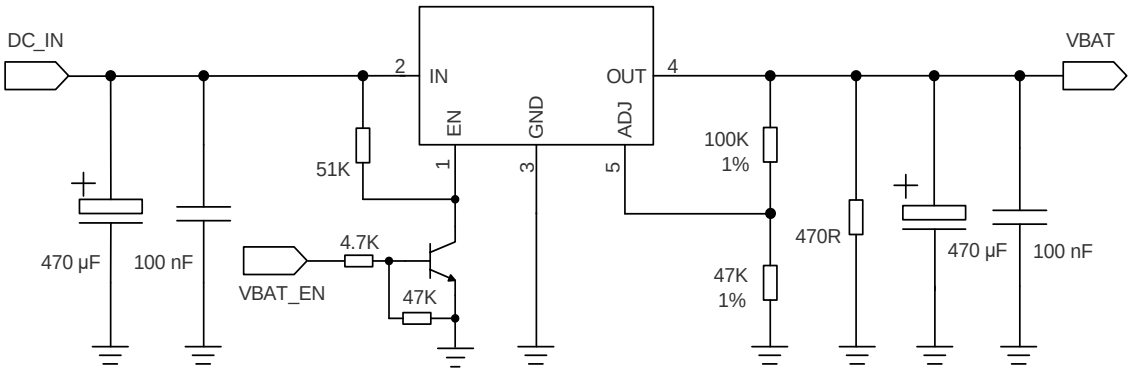


Figure 6: Reference Design of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Power Supply Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

3.4.4. Voltage Stability Requirements

The power supply of the module ranges from 3.3 to 4.5 V. Please ensure the input voltage never drops below 3.3 V.

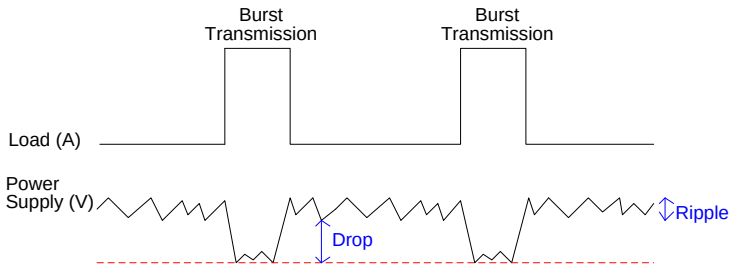


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, bypass capacitors of about 100 µF with low ESR should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use 4 ceramic capacitors (100 nF, 6.8 nF, 220 pF, 68 pF) for composing the MLCC

array for VABT_BB and 6 ceramic capacitors (100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for composing the MLCC array for VABT_RF, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be not less than 1 mm, and the width of VBAT_RF trace should be not less than 1.5 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to ensure the stability of the power supply, it is recommended to use a TVS with working peak reverse voltage of 5 V. The following figure shows the star structure of the power supply.

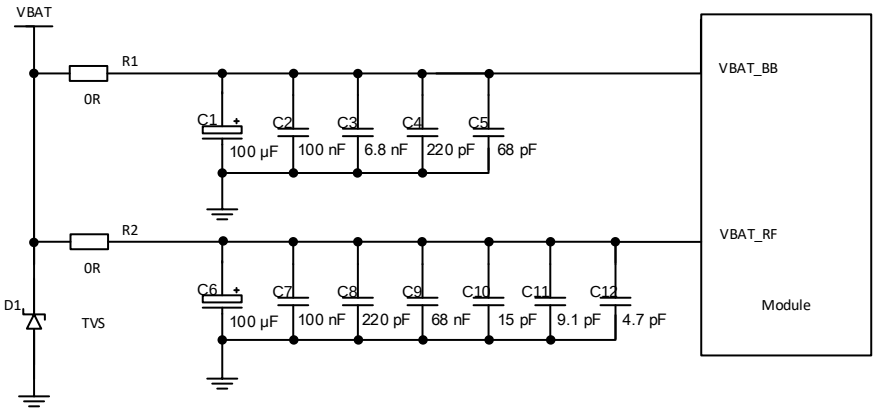


Figure 8: Star Structure of the Power Supply

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	171	DI	Turn on/off the module	Internally pulled up to 1.8 V. Active low.

When the module is in turn-off mode, it can be turned on and enter normal operation mode by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin outputs a high level, PWRKEY can be released. A simple reference circuit is illustrated in the following figure.

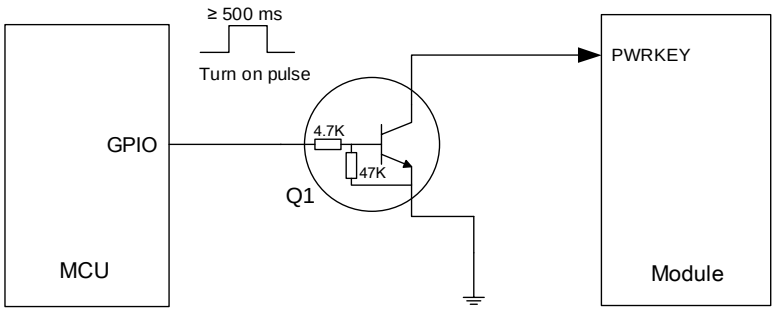


Figure 9: Turn On the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

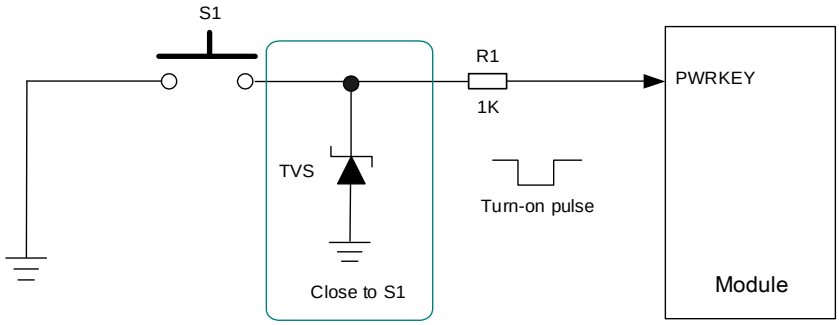


Figure 10: Turn On the Module Using a Button

The power-up scenario is illustrated in the following figure.

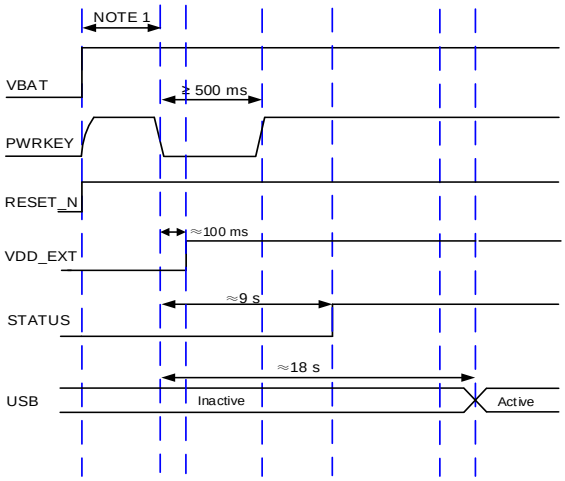


Figure 11: Power-up Timing

NOTE

1. Make sure that VBAT is stable for at least 60 ms before pulling down the PWRKEY pin.
2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if the module needs to be turned on automatically and shutdown is not needed.
3. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.5.2. Turn On with PON_1

Table 10: Pin Description of PON_1

Pin Name	Pin No.	I/O	Description	Comment
PON_1	173	DI	Turns on the module automatically when it is pulled high	Pull it up to 1.8–4.5 V. If unused, pull it down to GND.

3.6. Turn Off

Both driving the PWRKEY pin low and execute AT command can turn off the module normally.

3.6.1. Turn Off with PWRKEY

Drive the PWRKEY low for at least 800 ms, then the module will execute a power-down procedure after the PWRKEY is released. The power-down timing is illustrated in the following figure.

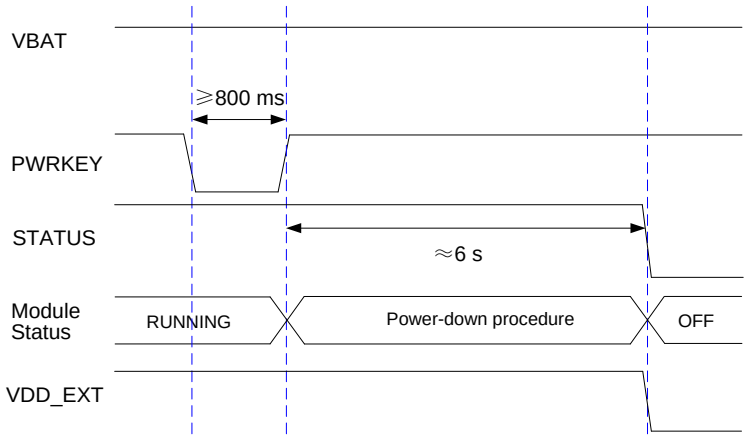


Figure 12: Power-down Timing

3.6.2. Turn off with AT Command

It is also a safe way to turn off the module with **AT+QPOWD**, which is similar to turn off the module via the PWRKEY pin. See details of **AT+QPOWD** in ***document [2]***.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with **AT+QPOWD**, keep PWRKEY at a high level after the execution of the command. Otherwise, the module will be turned on again after successful turn-off.

3.7. RESET_N

The module can be reset by driving the RESET_N low for 250–600 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	172	DI	Reset the module	Internally pulled up to 1.8 V. Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver can control the RESET_N.

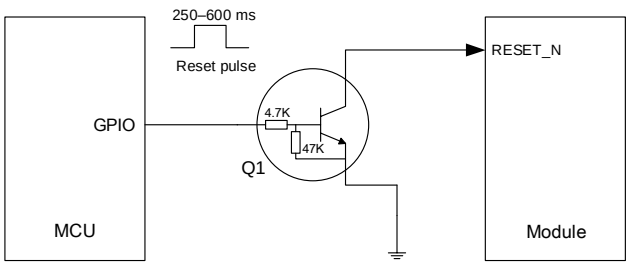


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

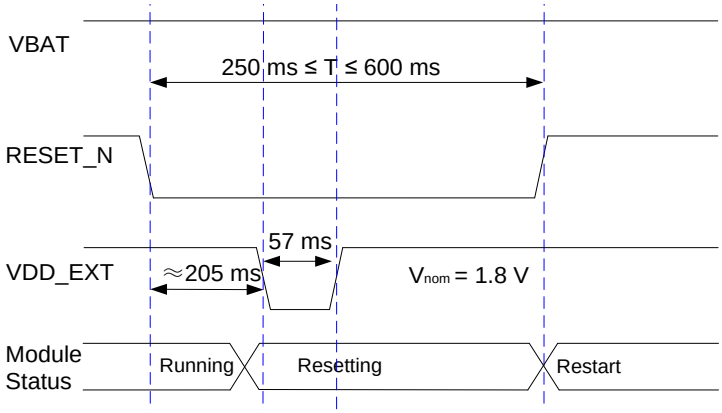


Figure 14: Reset Timing

NOTE

1. Use RESET_N only when it fails to be turned off with **AT+QPOWD** or the PWRKEY pin. See ***document [2]*** for details about **AT+QPOWD**.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0 and 2.0 specifications and supports SuperSpeed (5 Gbps) mode on USB 3.0 and high-speed (480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade, and voice* over USB.

Table 12: Functions of the USB Interface

Function	USB High-speed/Full-speed Interface
AT command communication	√
Data transmission	√
Software debugging	√
Firmware upgrade	√
Voice over USB*	√

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	182	AI	USB connection detect	For USB Connection detection only, not power supply. A test point must be reserved.
USB_ID*	179	DI	USB ID detect	
USB_DP	183	AIO	USB differential data (+)	Comply with USB 2.0 specifications. Require differential
USB_DM	184	AIO	USB differential data (-)	

				impedance of 90 Ω. Test points must be reserved.
USB_SS_TX_P	177	AO	USB 3.0 super-speed transmit (+)	Comply with USB 3.0 specifications. Require differential impedance of 90 Ω.
USB_SS_TX_M	175	AO	USB 3.0 super-speed transmit (-)	
USB_SS_RX_P	180	AI	USB 3.0 super-speed receive (+)	
USB_SS_RX_M	178	AI	USB 3.0 super-speed receive (-)	

Test points of the USB interface must be reserved, which can be used for software debugging and firmware upgrading in your designs. The following figure shows a reference circuit of USB interface.

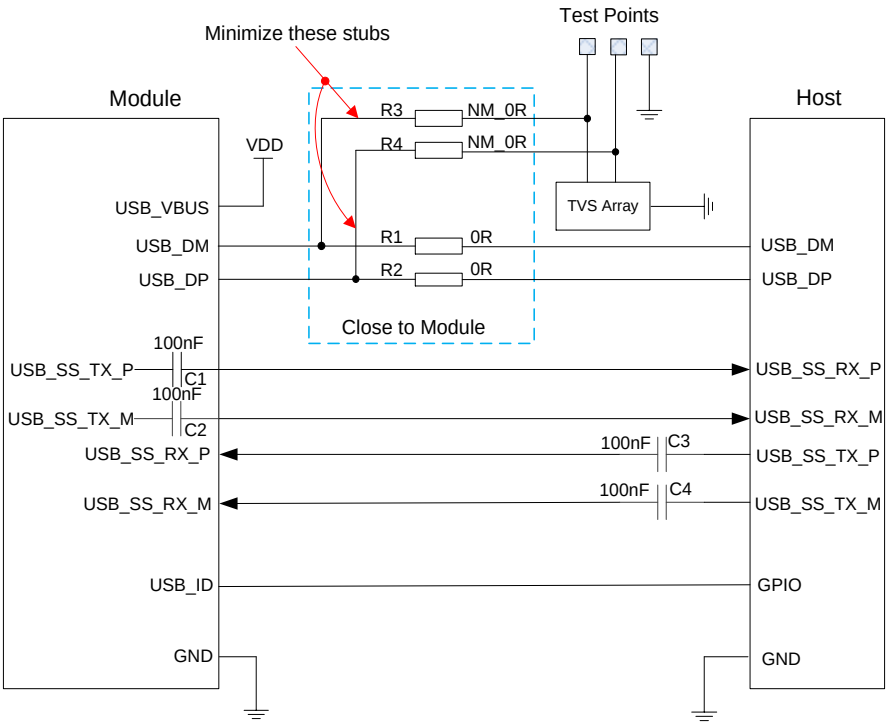


Figure 15: Reference Circuit of USB Interface

To ensure the signal integrity of USB data traces, C1, and C2 have already been integrated in the module; C3 and C4 must be placed close to the host; and R1 to R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles of USB interface should be followed during USB interface design to meet USB 2.0 and USB 3.0 specifications.

- Route the USB 2.0 and 3.0 signal traces as differential pair with ground surrounded. The impedance of USB differential trace is 90 Ω.

- For USB 2.0 signal traces, the trace should be shorter than 120 mm, and the differential data pair matching should be less than 2 mm. For USB 3.0 signal traces, the maximum length of each differential data pair (TX/RX) is recommended to be less than 100 mm, and each differential data pair matching should be less than 0.7 mm. While the matching between Tx and Rx should be less than 15.24 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is vital to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Keep the ESD protection devices as close to the USB connector as possible.
- Junction capacitance of the ESD protection components might cause influences on USB data lines, so pay attention to the selection of the component. Typically, the stray capacitance should be less than 2.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

Table 14: USB Trace Length Inside EG065K-NA

Pin No.	Signal Trace	Length (mm)	Length Difference (mm)
193	USB_DP	18.4	0.32
194	USB_DM	18.8	
177	USB_SS_TX_P	19.6	0.75
175	USB_SS_TX_M	18.8	
180	USB_SS_RX_P	17.8	0.16
178	USB_SS_RX_M	18.0	

Table 15: USB Trace Length Inside EG065K-EA

Pin No.	Signal Trace	Length (mm)	Length Difference (mm)
193	USB_DP	18.4	0.32
194	USB_DM	18.8	
177	USB_SS_TX_P	19.6	0.71
175	USB_SS_TX_M	18.9	
180	USB_SS_RX_P	17.8	0.16
178	USB_SS_RX_M	18.0	

4.2. PCIe Interface

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface. The PCIe interface of the module can transmit data. The module supports PCIe Root Complex (RC) mode only.

- *PCI Express Base Specification Revision 2.0* compliant
- Data rate up to 5 Gbps/lane
- Can be connected to an external Ethernet IC (MAC and PHY) or WLAN IC

Table 16: Pin Definition of the PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_ REFCLK_P	64	AO	PCIe reference clock (+)	Require differential impedance of 95 Ω. If unused, keep them open.
PCIE_ REFCLK_M	65	AO	PCIe reference clock (-)	
PCIE_TX_P	58	AO	PCIe transmit (+)	
PCIE_TX_M	59	AO	PCIe transmit (-)	
PCIE_RX_P	61	AI	PCIe receive (+)	
PCIE_RX_M	62	AI	PCIe receive (-)	
CLKREQ#	54	DI	PCIe clock request	It is an input signal. If unused, keep it open.
PERST#	55	DO	PCIe RC reset	It is an output signal. If unused, keep it open.
PEWAKE#	60	DI	PCIe wake up	It is an input signal. If unused, keep it open.

To enhance the reliability and availability in applications, follow the criteria below in the PCIe interface circuit design:

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and clock signals.
- Add a capacitor in series on Rx and Tx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx/REFCLK) less than 0.7 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as 85 Ω ±10 %.

You must not route PCIe data traces under components or cross them with other traces.

The module only supports Root Complex (RC) mode. In this mode, the module is configured to act as a PCIe RC device. The following figure shows a reference circuit of PCIe RC mode.

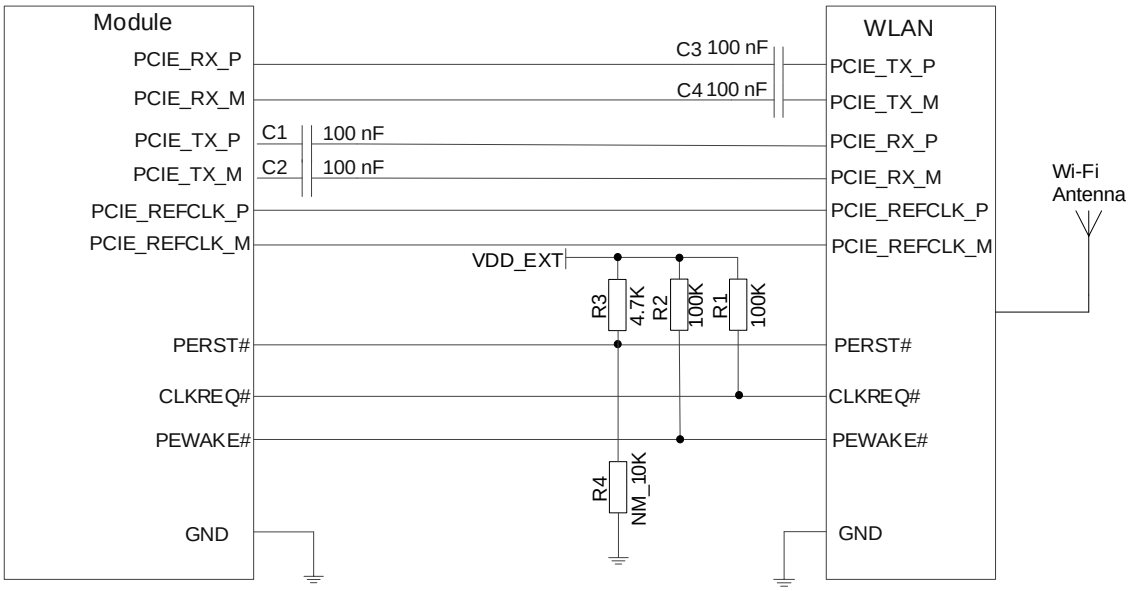


Figure 16: PCIe Interface Reference Circuit (RC Mode)

Table 17: PCIe Trace Length Inside EG065K-NA and EG065K-EA

Pin No.	Signal Trace	Length (mm)	Length Difference (mm)
64	PCIE_REFCLK_P	20.2	0.01
65	PCIE_REFCLK_M	20.2	
58	PCIE_TX_P	18.5	0.16
59	PCIE_TX_M	18.7	
61	PCIE_RX_P	18.5	0.08
62	PCIE_RX_M	18.5	

4.3. SDIO Interface*

The module provides one SDIO interface which supports SD 3.0 protocol and eMMC. The following table shows the pin definition.

Table 18: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_VDD	38	PO	**SD card application**: SDIO pull up power source **eMMC application**: Keep it open as used for eMMC	The module supports either 1.8 V or 3.0 V automatically. Cannot work as SD card power supply. SD card must be powered by an external power supply.
SDIO_PWR_EN	31	DO	SDIO power enable	If unused, keep them open.
SDIO_DET	32	DI	SD card detect	
SDIO_CMD	34	DIO	SDIO command	
SDIO_CLK	41	DO	SDIO clock	
SDIO_DATA0	36	DIO	SDIO data bit 0	
SDIO_DATA1	37	DIO	SDIO data bit 1	
SDIO_DATA2	39	DIO	SDIO data bit 2	
SDIO_DATA3	40	DIO	SDIO data bit 3	

The following figure shows an SDIO interface reference design.

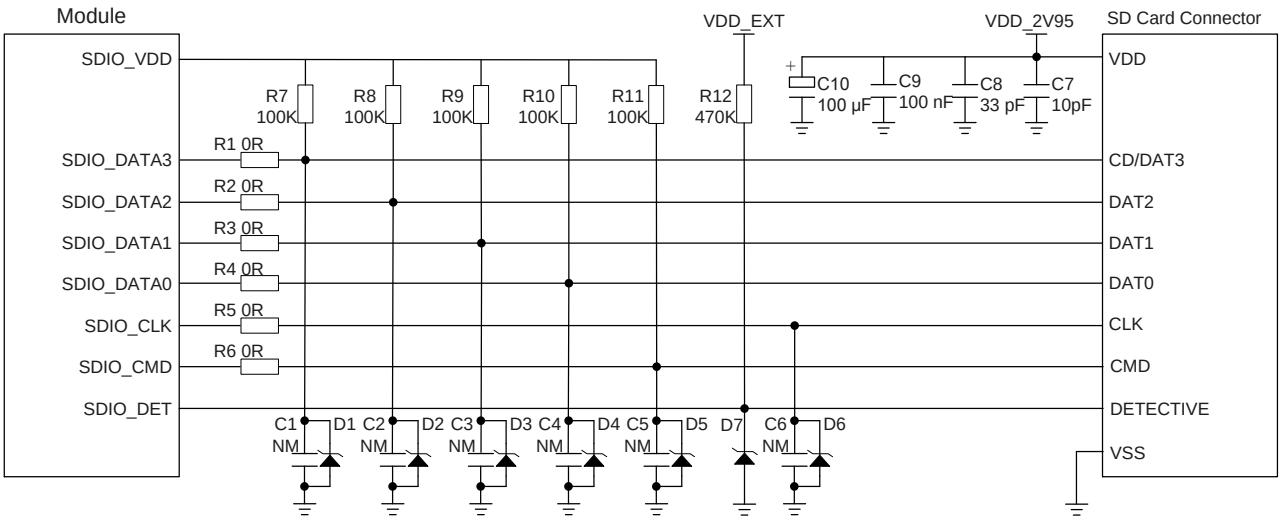


Figure 17: Reference Circuit of SD Card Application

Please follow the principles below in the SD card circuit design:

- The voltage range of SD power supply is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SDIO_VDD is 50 mA which can only be used as SDIO pull-up resistors, an external power supply is needed for SD card.
- To avoid jitter of bus, resistors R7 to R11 work to pull up the SDIO to SDIO_VDD. Values of these resistors range from 10 to 100 kΩ and the preferred value is 100 kΩ.
- To improve signal quality, it is recommended to add 0 Ω resistors R1 to R6 in series between the module and the SD card connector. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- For better ESD protection, it is recommended to add a TVS on each SD signal trace.
- It is important to route the SDIO signal traces at inner layer with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noise signals such as clock signals and DC-DC signals.
- It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA /SDIO_CMD within 1 mm and the total routing length less than 50 mm. The traces inside the module are 10 mm long in total, so the exterior traces should be less than 40 mm in total.
- Ensure the adjacent trace spacing is twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.

4.4. USB_BOOT

Table 19: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	30	DI	Force the module into emergency download mode	Active high. A test point is recommended to be reserved.

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before turning on the module, thus the module will enter emergency download mode after being turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

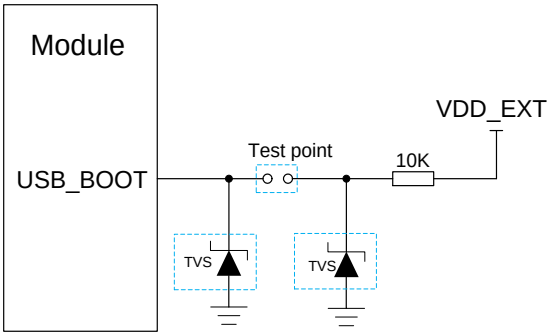


Figure 18: Reference Circuit of USB_BOOT Interface

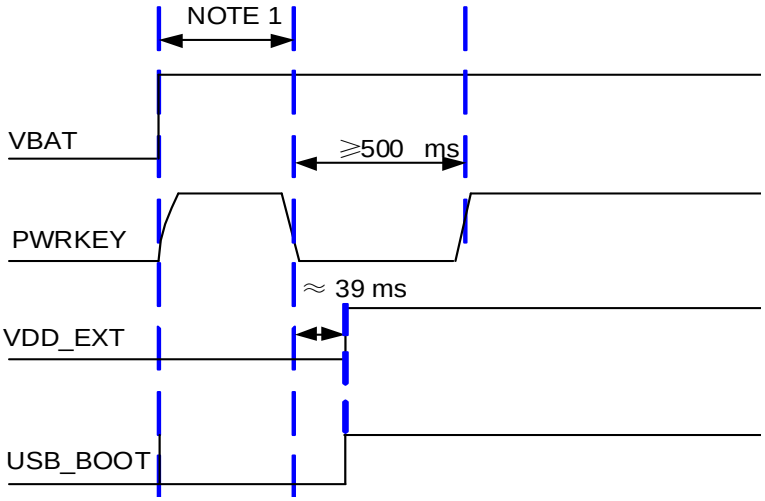


Figure 19: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 60 ms.
2. When using MCU to control the module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Connect the test points as shown in ***Figure 18*** can manually force the module to enter emergency download mode.

4.5. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported, and Dual (U)SIM Single Standby function is supported.

Table 20: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	139	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	138	DIO	(U)SIM1 card data	
USIM1_CLK	141	DO	(U)SIM1 card clock	
USIM1_RST	142	DO	(U)SIM1 card reset	
USIM1_DET	143	DI	(U)SIM1 card hot-plug detect	If unused, keep it open.
USIM2_VDD	148	PO	(U)SIM2 card power supply	If (U)SIM2 interface is unused, keep it open.
USIM2_DATA	144	DIO	(U)SIM2 card data	If (U)SIM2 interface is unused, keep it open.
USIM2_CLK	147	DO	(U)SIM2 card clock	If (U)SIM2 interface is unused, keep it open.
USIM2_RST	145	DO	(U)SIM2 card reset	If (U)SIM2 interface is unused, keep it open.
USIM2_DET	146	DI	(U)SIM2 card hot-plug detect	If (U)SIM2 interface is unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pin. The function supports low and high level detections, and the detection is at low level by default. You can use **AT+QSIMDET** to change the detect level or disable the function of hot-plug. See ***document [2]*** for details about **AT+QSIMDET**.

Normally Closed (U)SIM Card Connector:

- When the (U)SIM is absent, CD is short-circuited to ground and USIM_DET is at low level.
- When the (U)SIM is inserted, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design of (U)SIM interface with a normally closed (NC) 8-pin (U)SIM card connector.

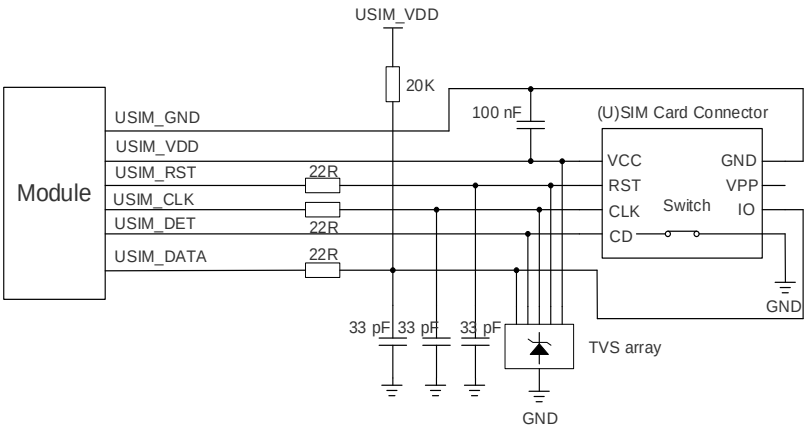


Figure 20: Reference Circuit of Normally Closed (U)SIM Card Connector

Normally Open (U)SIM Card Connector:

- When the (U)SIM is absent, CD is open from ground and USIM_DET is at high level.
- When the (U)SIM is inserted, CD is short-circuited to ground and USIM_DET is at low level.

If (U)SIM card detection function is not needed, please keep USIM_DET open.

The following figure illustrates a reference design for (U)SIM card interface with a normally open (NO) 8-pin (U)SIM card connector.

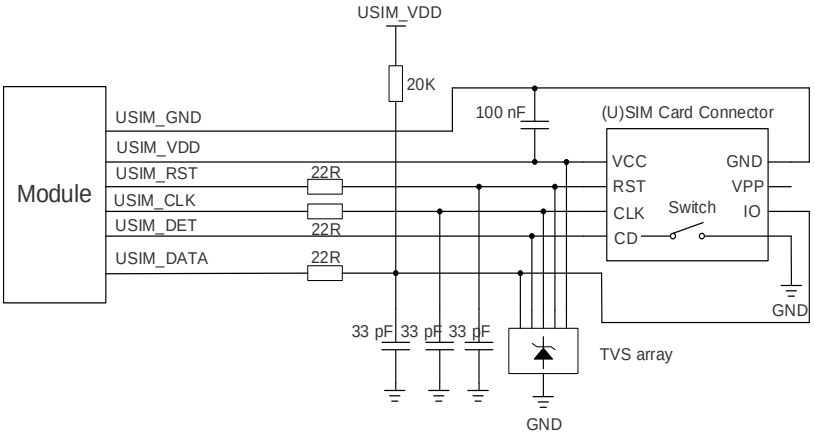


Figure 21: Reference Circuit of Normally Open (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as short as possible, 200 mm at most.
- Keep (U)SIM card signal traces away from RF and VBAT traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- For better ESD protection, it is recommended to add a TVS array with a parasitic capacitance not exceeding 50 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. These 33 pF capacitors are used to filter out RF interference.
- The pull-up resistor on USIM_DATA trace improves anti-jamming capability and should be placed close to the (U)SIM card connector.
- (U)SIM card hot-plug function is supported by default.

4.6. UART Interface

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps (default), 230400 bps, 460800 bps and 921600 bps baud rates. It also supports RTS

and CTS hardware flow control, and can be used for data transmission and AT command communication.

- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

4.6.1. Main UART Interface

Table 21: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RXD	77	DI	Main UART receive	If unused, keep them open.
MAIN_TXD	79	DO	Main UART transmit	
MAIN_RTS	80	DI	Request to send signal to the module	RTS: Connect to the MCU's RTS. CTS: Connect to the MCU's CTS.
MAIN_CTS	82	DO	Clear to send signal from the module	
MAIN_DCD	86	DO	Main UART data carrier detect	If unused, keep them open.
MAIN_RI	83	DO	Main UART ring indication	
MAIN_DTR	85	DI	Main UART data terminal ready	Pulled up by default. Pulling low will awaken the module. If unused, keep it open. Sleep mode control.

4.6.2. Debug UART Interface

Table 22: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	88	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	89	DO	Debug UART transmit	

4.6.3. UART Application

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas

Instruments is recommended. The following figure shows a reference design.

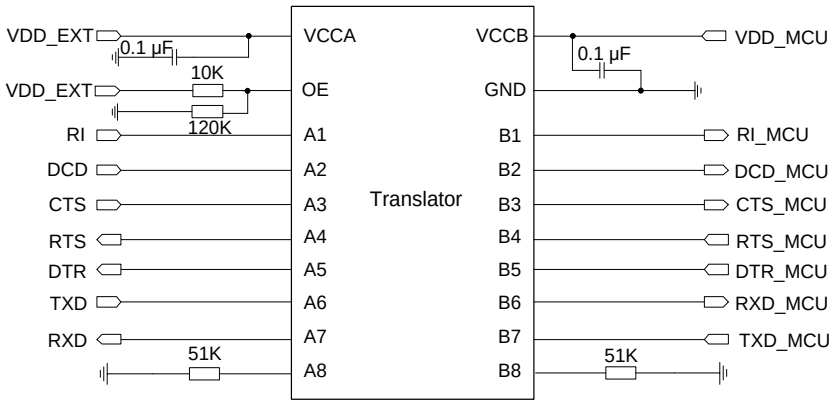


Figure 22: Level-shifting Circuit (IC Solution)

Please visit http://www.ti.com for more information.

Another example with level-shifting circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

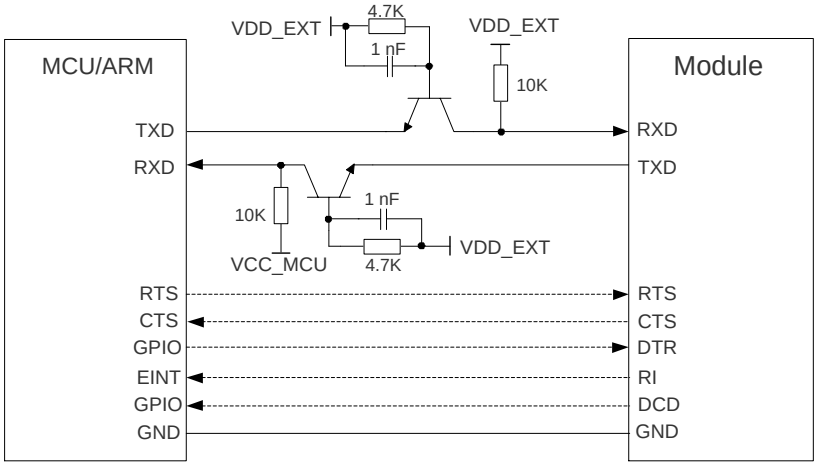


Figure 23: Level-shifting Circuit (Transistor Solution)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.

4.7. SPI *

The module provides one SPI which only supports master mode with a maximum clock frequency up to 50 MHz.

Table 23: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_MOSI	1	DO	SPI master-out slave-in	1.8 V power domain. Master mode only. If unused, keep them open.
SPI_CLK	4	DO	SPI clock	
SPI_MISO	3	DI	SPI master-in slave-out	
SPI_CS	2	DO	SPI chip select	

4.8. I2C Interfaces*

The module provides one I2C interface. As an open drain output, it should be pulled up to 1.8 V.

Table 24: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SDA	29	OD	I2C serial data (for external codec)	Pull each of them up to VDD_EXT with an external 4.7 kΩ resistor. If unused, keep them open.
I2C_SCL	26	OD	I2C serial clock (for external codec)	

4.9. PCM Interface*

The module supports audio communication via Pulse Code Modulation (PCM) digital interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave
- Auxiliary mode (long frame synchronization): the module works as master only

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, when PCM_SYNC is at 8 kHz, PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz, whereas it also supports 4096 kHz when PCM_SYNC is at 16 kHz.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. PCM_CLK supports 256 kHz when PCM_SYNC is at 8 kHz with a 50 % duty cycle.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

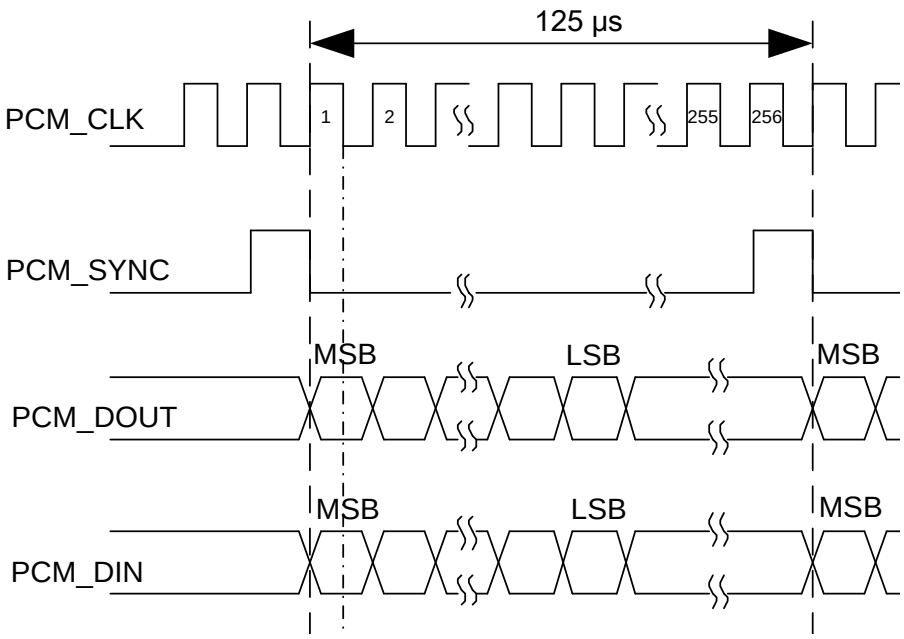


Figure 24: Primary Mode Timing

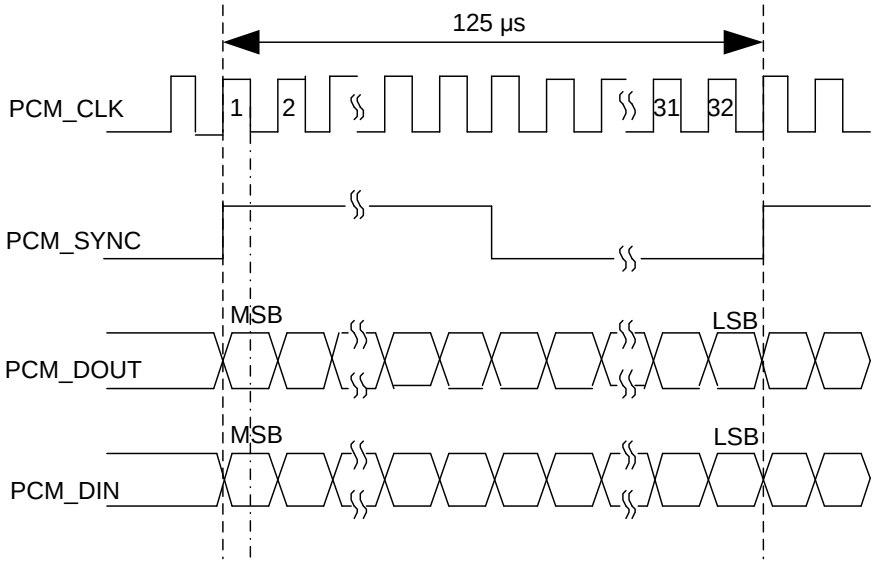


Figure 25: Auxiliary Mode Timing

The following table shows the pin definition of PCM interface.

Table 25: Pin Definition of PCM interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	7	DIO	PCM data frame sync	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_DIN	9	DI	PCM data input	If unused, keep it open.
PCM_CLK	10	DIO	PCM clock	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_ DOUT	12	DO	PCM data output	If unused, keep it open.

Clock and mode can be configured by **AT+QDAI**, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [2]*** for details about the AT command.

The following figure shows a reference design of PCM and I2C interface with an external codec IC.

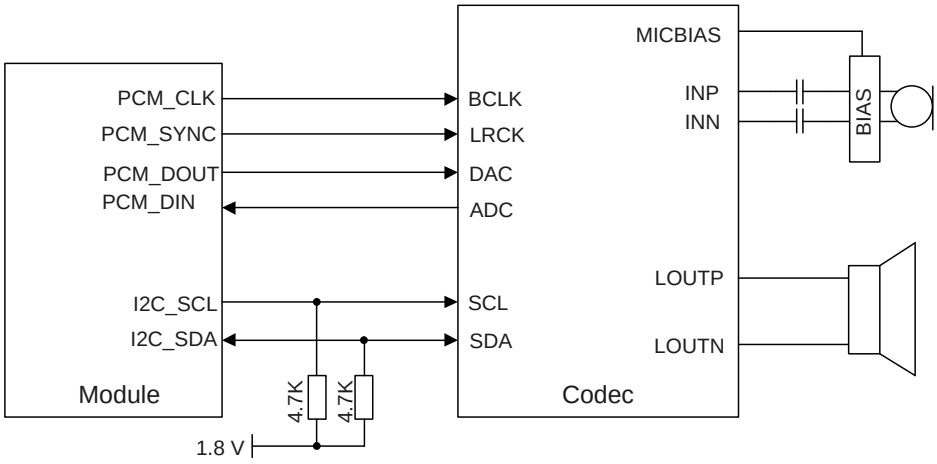


Figure 26: Reference Circuit of PCM Application with Audio Codec

The following figure shows a reference design of PCM and SPI interface with an external SLIC IC. The dotted lines in the table below mean an optional connection since some SLIC ICs need INT and RST while some do not.

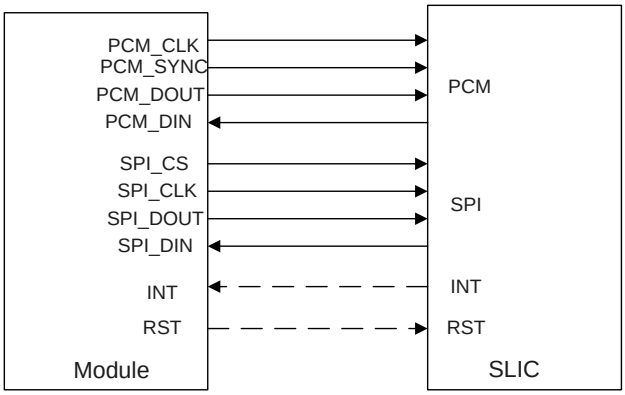


Figure 27: Reference Circuit of PCM and SPI Application with SLIC

4.10. I2S Interface*

The module provides one I2S interface. Pin definition is here as follows:

Table 26: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
I2S_WS	45	DIO	I2S word select	In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_SCK	44	DIO	I2S clock	In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_DIN	47	DI	I2S data in	If unused, keep them open.
I2S_DOUT	46	DO	I2S data out	
MCLK	49	DO	Clock output for codec	
EXT_RST	52	DO	External audio reset	
EXT_INT	50	DI	External audio interrupt	

The following figure shows a reference design of I2S interface with an external codec IC. The dotted line in the table below means an optional connection since some Codec ICs need MCLK while some do not

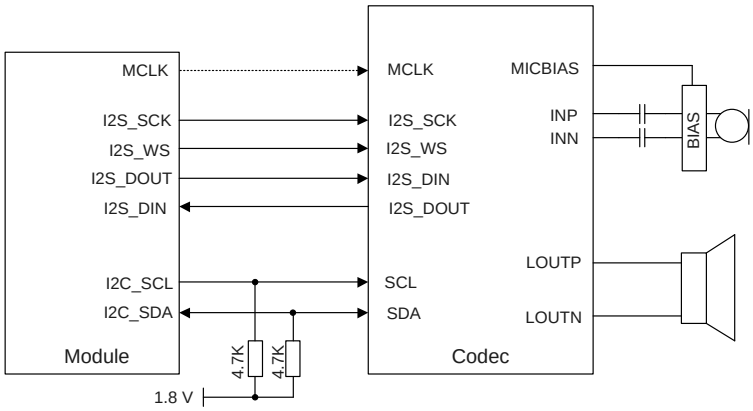


Figure 28: Reference Circuit of I2S Application with Audio Codec

4.11. ADC Interface

The module provides one Analog-to-Digital Converter (ADC) interface. To improve the accuracy of ADC, the interface trace should be surrounded by ground.

Table 27: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC	18	AI	General-purpose ADC interface	If unused, keep it open.

The voltage value on the pin ADC can be read via **AT+QADC=<port>**. For more details about the AT command, see ***document [2]***.

The following table describes the characteristics of the ADC interface.

Table 28: Characteristics of ADC Interface

Characteristics	Min.	Typ.	Max.	Unit
Voltage Range	0	-	1.875	V
Input Resistance	10	-	-	MΩ
Resolution	-	14	-	bits
Sample Rate	-	4.8	-	MHz

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT power supply is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

4.12. Indication Signals

Table 29: Pin Definition of Indication Interface

Pin Name	Pin No.	I/O	Description	Comment
STATUS	24	DO	Indicate the module's operation status	If unused, keep them open.
SLEEP_IND	23	DO	Indicate the module's sleep mode	
NET_MODE	25	DO	Indicate the module's network registration mode	
NET_STATUS	27	DO	Indicate the module's network activity status	

4.12.1. STATUS

The STATUS pin is an output pin for indicating the module's operation status. It will output high level when module is turned on successfully. A reference circuit is shown as below.

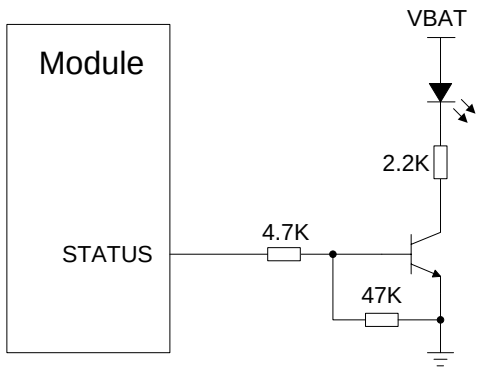


Figure 29: Reference Circuit of STATUS

4.12.2. SLEEP_IND

The SLEEP_IND pin is an output pin, indicating the module's sleep mode. It will output high level when the module enters sleep mode. A reference circuit is shown as below.

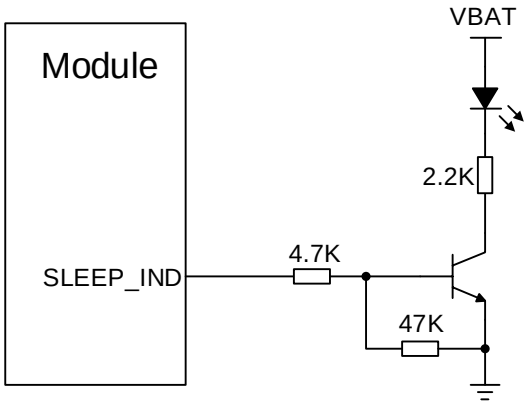


Figure 30: Reference Circuit of SLEEP_IND

4.12.3. Network Status Indication

The network indication pins NET_MODE and NET_STATUS can drive network status indicators. The following table describes the pin definition and logic level changes in different network status.

Table 30: Working State of Network Connection Status/Activity Indication

Pin Name	Status	Description
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

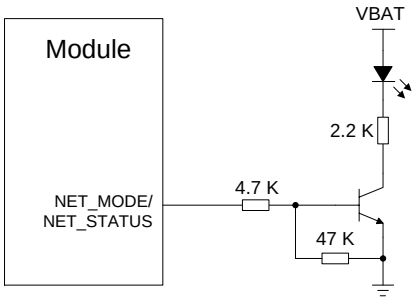


Figure 31: Reference Circuit of Network Status Indication

4.13. W_DISABLE#

The module provides a W_DISABLE# pin to enable or disable airplane mode through hardware operation. W_DISABLE# is pulled up by default, and driving it low will set the module to airplane mode. In airplane mode, the RF function will be disabled.

Table 31: Pin Definition of W_DISABLE#

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	90	DI	Airplane mode control	Pulled up by default. At low voltage level, the module will enter airplane mode. If unused, keep it open.

The RF function can also be enabled or disabled through software AT commands. See ***document [2]*** for details of **AT+CFUN=<fun>**.

Table 32: RF Function Status

W_DISABLE# Logic Level	AT Command	RF Function Status	Operating Mode
High Level	**AT+CFUN=1**	Enable	Full functionality mode
	AT+CFUN=0	Disable	Minimum functionality mode
	AT+CFUN=4	Disable	Airplane mode
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disable	Airplane mode

4.14. DPR

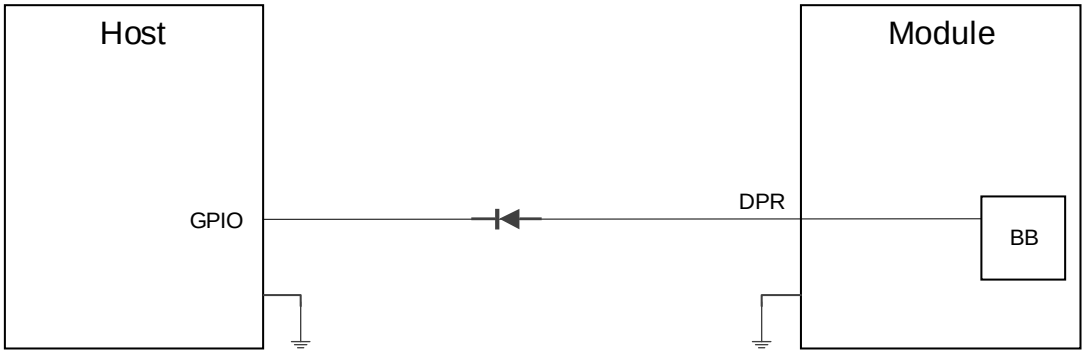
The module provides a DPR (Dynamic Power Reduction) pin for body SAR (Specific Absorption Rate) detection. The signal is sent by a host system proximity sensor to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 33: Pin Definition of DPR

Pin Name	Pin No.	I/O	Description	Comment
DPR	15	DI	Dynamic power reduction	Active low.

Table 34: Function of the DPR

DPR Level	Function
High/Floating	Max transmitting power will not be backed off
Low	Max transmitting power will be backed off



NOTE: DPR pin is 1.8 V power domain. Host's GPIO could be a 1.8 V or 3.3 V voltage level.

Figure 32: Reference Circuit of DPR

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Antenna Interface & Frequency Bands

Table 35: Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN1	98	AIO	Main antenna interface LTE LMB_TRX ● For EG065K-NA, LMB includes B2/B4/B5/B12/B13/B14/B25/B26/B66 ● For EG065K-EA, LMB includes B1/B2/B3/B4/B5/B8/B20/B28 WCDMA LMB_TRX ● For EG065K-NA, LMB includes B2/B4/B5 ● For EG065K-EA, LMB includes B1/B2/B3/B4/B5/B8	50 Ω impedance.
ANT_MAIN2	107	AIO	Main antenna interface LTE HB_TRX ● For EG065K-NA, HB includes B7/B30 ● For EG065K-EA, HB includes B7/B40	
ANT_DRX1	125	AI	Diversity antenna interface LTE MHB_DRX ● For EG065K-NA, MHB includes B2/B4/B7/B25/B30/B66 ● For EG065K-EA, MHB includes B1/B2/B3/B4/B7/B40 WCDMA MB_DRX ● For EG065K-NA, MB includes B2/B4 ● For EG065K-EA, MB includes B1/B2/B3/B4	

ANT_DRX2	133	AI	Diversity antenna interface LTE LB_DRX ● For EG065K-NA, LB includes B5/B12/B13/B14/ B26 ● For EG065K-EA, LB includes B5/B8/B20/B28/ WCDMA LB_DRX ● For EG065K-NA, LB includes B5 ● For EG065K-EA, LB includes B5/B8

NOTE

Only passive antennas are supported.

Table 36: Operating Frequency of EG065K-NA

Operating Frequency	Transmit (MHz)	Receive (MHz)
WCDMA B2	1850–1910	1930–1990
WCDMA B4	1710–1755	2110–2155
WCDMA B5	824–849	869–894
LTE B2	1850–1910	1930–1990
LTE B4	1710–1755	2110–2155
LTE B5	824–849	869–894
LTE B7	2500–2570	2620–2690
LTE B12	699–716	729–746
LTE B13	777–787	746–756
LTE B14	788–798	758–768
LTE B25	1850–1915	1930–1995
LTE B26	814–849	859–894
LTE B30	2305–2315	2350–2360
LTE B66	1710–1780	2110–2200

Table 37: Operating Frequency of EG065K-EA

Operating Frequency	Transmit (MHz)	Receive (MHz)
WDCMA B1	1920–1980	2110–2170
WDCMA B2	1850–1910	1930–1990
WDCMA B3	1710–1785	1805–1880
WDCMA B4	1710–1755	2110–2155
WDCMA B5	824–849	869–894
WDCMA B8	880–915	925–960
LTE B1	1920–1980	2110–2170
LTE B2	1850–1910	1930–1990
LTE B3	1710–1785	1805–1880
LTE B4	1710–1755	2110–2155
LTE B5	824–849	869–894
LTE B7	2500–2570	2620–2690
LTE B8	880–915	925–960
LTE B20	832–862	791–821
LTE B28	703–748	758–803
LTE B40	2300–2400	2300–2400

5.2. Antenna Tuner Control Interface

5.2.1. Antenna Tuner Control Interface through RFFE

Table 38: Pin Definition of Antenna Tuner Control Interface through RFFE

Pin Name	Pin No.	I/O	Description	Comment
RFFE5_CLK	66	DO	Used for external MIPI IC control	If unused, keep them open.
RFFE5_DATA	69	DIO	Used for external MIPI IC control	

5.2.2. Antenna Tuner Control Interface through GRFC

Table 39: Pin Definition of Antenna Tuner Control Interface through GRFC Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC2	118	DO	Generic RF controller	1.8 V	If unused, keep them open.
GRFC3	121	DO	Generic RF controller		
GRFC0	103	DO	Generic RF controller		
GRFC1	106	DO	Generic RF controller		

Table 40: Truth Table of GRFC Interfaces for EG065K-NA

GRFC6 Level	GRFC1 Level	GRFC34 Level	GRFC33 Level	Band
TBD	TBD	TBD	TBD	WCDMA B2
TBD	TBD	TBD	TBD	WCDMA B4
TBD	TBD	TBD	TBD	WCDMA B5
High	Low	High	Low	LTE-FDD B12
High	High	High	High	LTE-FDD B13
Low	High	Low	High	LTE-FDD B14
Low	Low	Low	Low	LTE-FDD B5
Low	Low	Low	Low	LTE-FDD B26
Low	Low	Low	Low	LTE-FDD B4
Low	Low	Low	Low	LTE-FDD B25
Low	Low	Low	Low	LTE-FDD B2
Low	Low	Low	Low	LTE-FDD B66
Low	Low	Low	Low	LTE-FDD B30
Low	Low	Low	Low	LTE-FDD B7

Table 41: Truth Table of GRFC Interfaces for EG065K-EA

GRFC6 Level	GRFC1 Level	GRFC34 Level	GRFC33 Level	Band
TBD	TBD	TBD	TBD	WCDMA B1
TBD	TBD	TBD	TBD	WCDMA B2
TBD	TBD	TBD	TBD	WCDMA B3
TBD	TBD	TBD	TBD	WCDMA B4
TBD	TBD	TBD	TBD	WCDMA B5
TBD	TBD	TBD	TBD	WCDMA B8
High	Low	High	Low	LTE-FDD B28
High	High	High	High	LTE-FDD B20
Low	High	Low	High	LTE-FDD B5
Low	Low	Low	Low	LTE-FDD B8
Low	Low	Low	Low	LTE-FDD B3
Low	Low	Low	Low	LTE-FDD B4
Low	Low	Low	Low	LTE-FDD B2
Low	Low	Low	Low	LTE-FDD B1
Low	Low	Low	Low	LTE-TDD B40
Low	Low	Low	Low	LTE-FDD B7

NOTE

Low level means “V_{OL}”; High level means “V_{OH}”

5.3. Tx Power

Table 42: Tx Power

Frequency Band	Max. Tx Power	Min. Tx Power
LTE FDD B30	22.3 dBm ±2 dB	< -40 dBm
LTE FDD Other bands	23.5 dBm ±2 dB	< -40 dBm
LTE TDD bands		
WCDMA Bands	23 dBm ±2 dB	< -40 dBm

5.4. Rx Sensitivity

Table 43: Rx Sensitivity of EG065K-NA

Frequency（10 MHZ）	Rx Sensitivity (Typ.)			3GPP (SIMO) (dBm)
	Primary (dBm)	Diversity (dBm)	SIMO (dBm)	
WCDMA B2	TBD	TBD	TBD	-104.7
WCDMA B4	TBD	TBD	TBD	-106.7
WCDMA B5	TBD	TBD	TBD	-104.7
LTE-FDD B2	-98	-99	-101	-94.3
LTE-FDD B4	-97.5	-99	-100.5	-96.3
LTE-FDD B5	-97.5	-100.3	-101	-94.3
LTE-FDD B7	-97	-97.3	-100	-94.3
LTE-FDD B12	-98	-101	-102.3	-93.3
LTE-FDD B13	-97.5	-100.3	-102	-93.3
LTE-FDD B14	-96.5	-100	-101.5	-93.3
LTE-FDD B25	-98	-98.3	-101	-92.8
LTE-FDD B26	-97.5	-100	-101	-93.8
LTE-FDD B30	-97.3	-97	-99.5	-95.3
LTE-FDD B66	-97.5	-98.5	-100.5	-95.8

Table 44: Rx Sensitivity of EG065K-EA

Frequency (10 MHZ)	Rx Sensitivity (Typ.)			3GPP (SIMO) (dBm)
	Primary (dBm)	Diversity (dBm)	SIMO (dBm)	
WCDMA B1	TBD	TBD	TBD	-106.7
WCDMA B2	TBD	TBD	TBD	-104.7
WCDMA B3	TBD	TBD	TBD	-103.7
WCDMA B4	TBD	TBD	TBD	-106.7
WCDMA B5	TBD	TBD	TBD	-104.7
WCDMA B8	TBD	TBD	TBD	-103.7
LTE-FDD B1	-96.5	-98.5	-100	-96.3
LTE-FDD B2	-97.5	-98	-100	-94.3
LTE-FDD B3	-96.7	-98	-100	-93.3
LTE-FDD B4	-97.3	-98.5	-100.2	-96.3
LTE-FDD B5	-97	-100.5	-102	-94.3
LTE-FDD B7	-97.3	-98.5	-100	-94.3
LTE-FDD B8	-96.2	-99.5	-102	-93.3
LTE-FDD B20	-98	-98	-101	-93.3
LTE-FDD B28	-98	-99.5	-101.5	-94.8
LTE-TDD B40	-96.5	-98.2	-99.5	-96.3

5.5. Reference Design

The module provides four RF antenna interfaces for antenna connection.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1, R2, R3, R4, C1, C2, C3, C4, C5, C6, C7 and C8) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

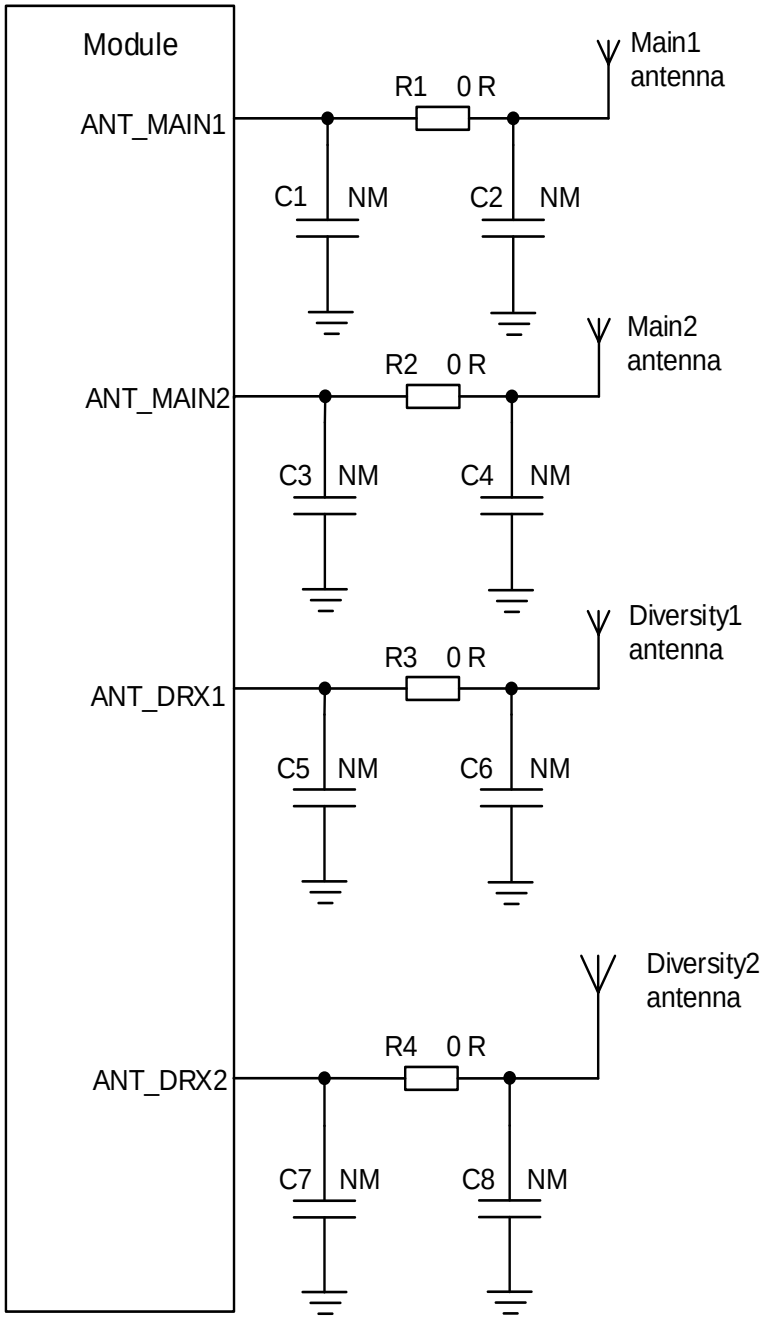


Figure 33: Reference Circuit for RF Antenna Interfaces

5.6. RF Routing Guidelines

When designing a PCB, characteristic impedance of all RF traces should be controlled to 50 Ω. In general, the impedance of RF traces is determined by materials' dielectric constant, trace width (W), spacing between RF traces and ground (S) and height from the reference ground to the signal layer (H). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures when characteristic impedance of RF traces is controlled to 50 Ω.

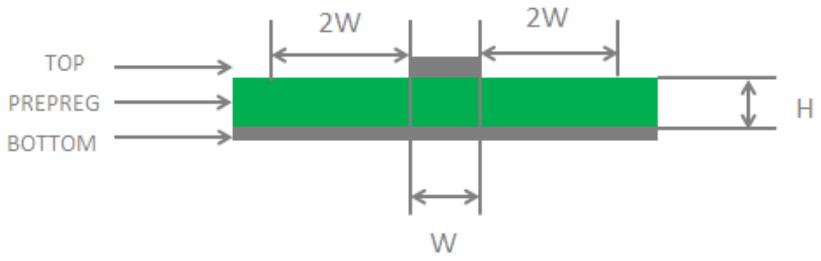


Figure 34: Microstrip Design on a 2-layer PCB

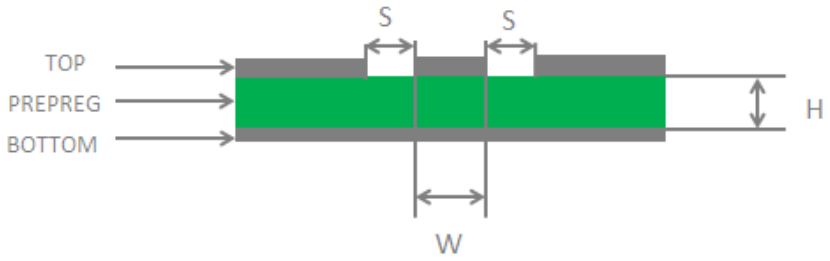


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

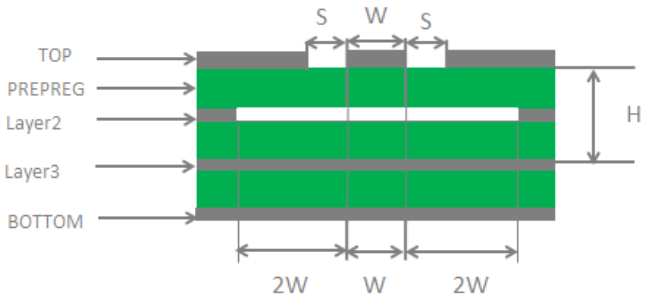


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

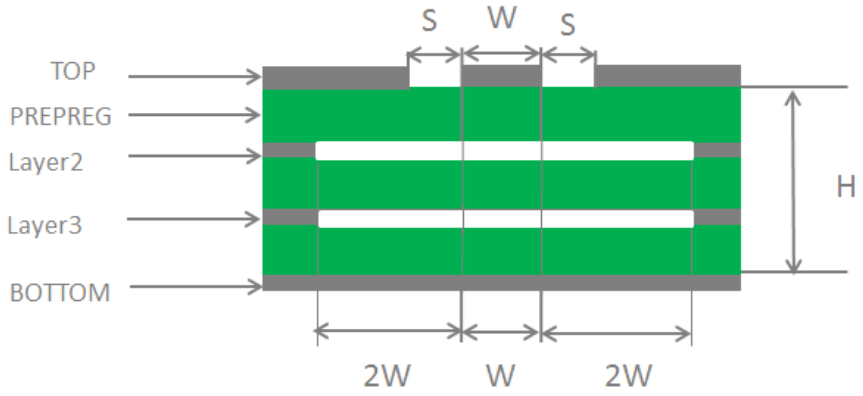


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure better RF performance and reliability, the following conditions should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to the ground plane.
- Distance between RF pins and RF connector should be as short as possible, and all right-angle (90°) traces should be replaced with 135° angle traces.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. However, ground vias around RF traces and the reference ground can improve RF performance. The distance between ground vias and RF traces should be at least two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.7. Antenna Design Requirements

Table 45: Requirements for Antenna Design

Antenna Type	Requirements
LTE and WCDMA	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.8. RF Connector Recommendation

The receptacle dimensions are illustrated as below.

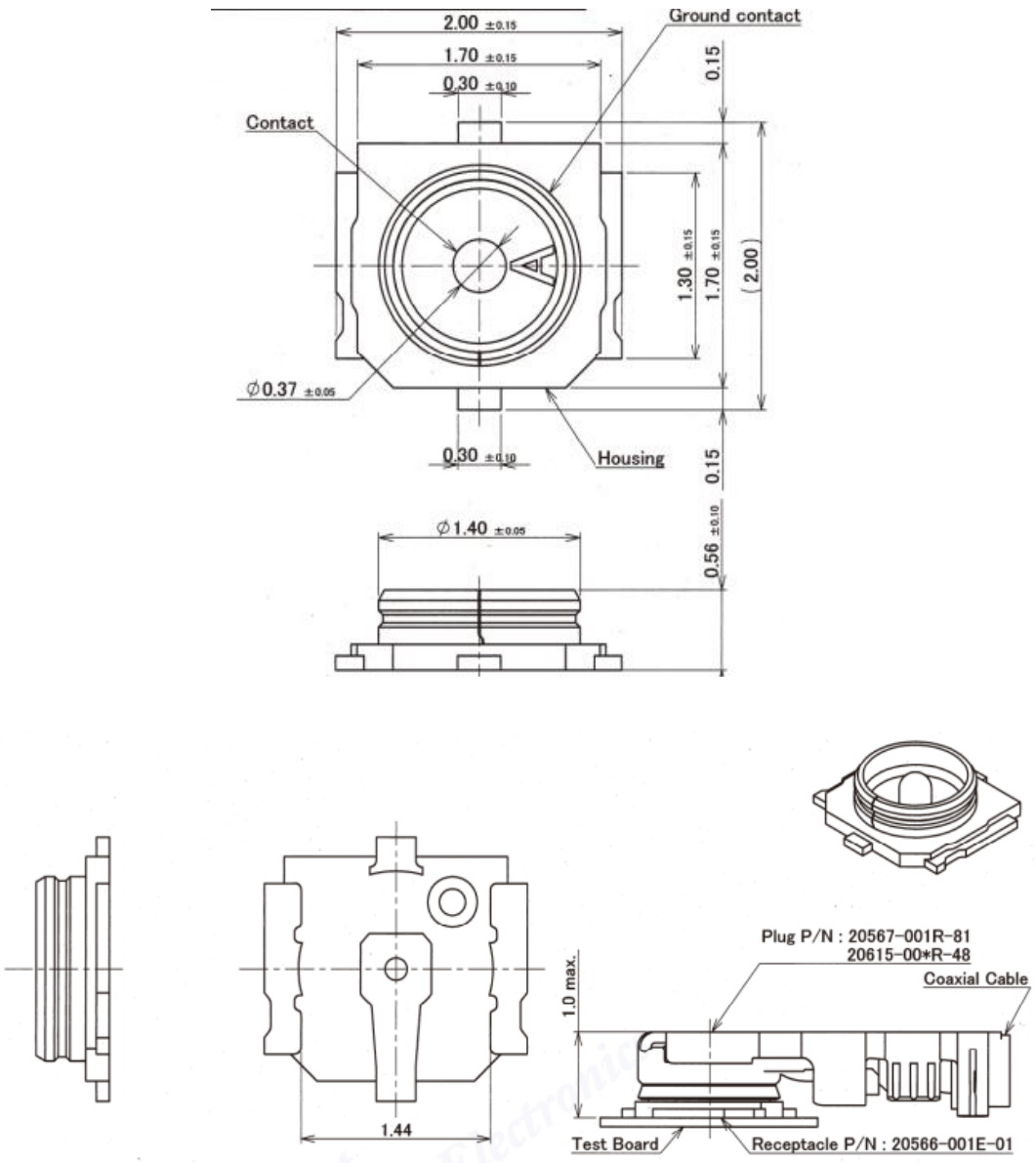


Figure 38: Dimensions of the Receptacle (Unit: mm)

The following figure describes the space factor of mated connector.

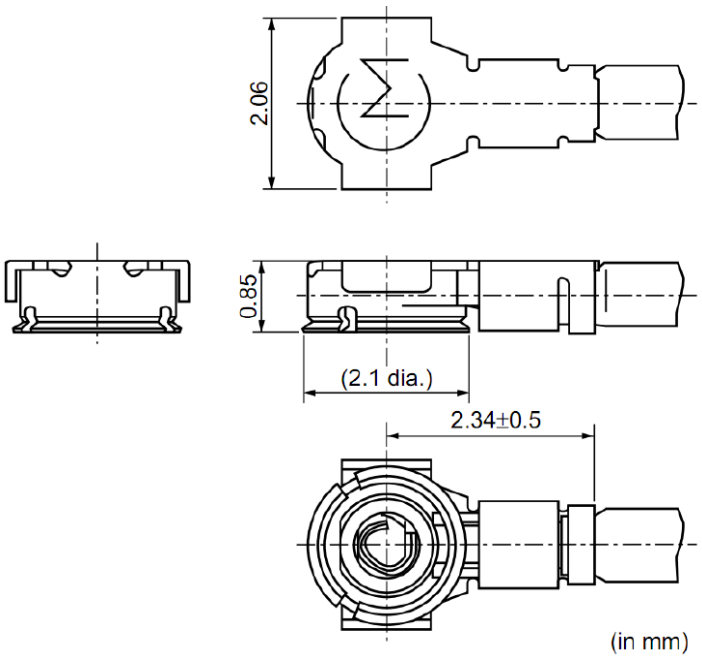


Figure 39: Dimensions of Mated Plugs (Ø0.81/Ø1.13 mm Coaxial Cables) (Unit: mm)

For more details, please visit https://www.i-pex.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 46: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.2	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC	-0.5	1.875	V

6.2. Power Supply Ratings

Table 47: Module Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.5	V
USB_VBUS	USB connection detection		3.3	5.0	5.25	V

6.3. Power Consumption

Table 48: EG065K-NA Power Consumption

Description	Condition	Typ.	Unit
OFF State	Power off	23	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.26	mA
	LTE-FDD @ DRX = 0.32 s	4.00	mA
	LTE-FDD @ DRX = 0.64 s	2.76	mA
	LTE-FDD @ DRX = 0.64 s (USB suspended)	3.08	mA
	LTE-FDD @ DRX = 1.28 s	2.10	mA
	LTE-FDD @ DRX = 2.56 s	1.79	mA
	WCDMA	TBD	mA
Idle state	LTE-FDD @ DRX = 0.64 s	11.48	mA
	LTE-FDD @ DRX = 0.64 s (USB active)	18.30	mA
	WCDMA	TBD	mA
WCDMA data transfer	WCDMA B2	TBD	mA
	WCDMA B4	TBD	mA
	WCDMA B5	TBD	mA
LTE data transfer	LTE-FDD B2 CH900 @ 23.5 dBm	545	mA
	LTE-FDD B4 CH2175 @ 23.5 dBm	545	mA
	LTE-FDD B5 CH2525 @ 23.5 dBm	590	mA
	LTE-FDD B7 CH3100 @ 23.5 dBm	760	mA
	LTE-FDD B12 CH5095 @ 23.5 dBm	590	mA
	LTE-FDD B13 CH5230 @ 23.5 dBm	660	mA
	LTE-FDD B14 CH5330 @ 23.5 dBm	630	mA
	LTE-FDD B25 CH8365 @ 23.5 dBm	550	mA
	LTE-FDD B26 CH8865 @ 23.5 dBm	645	mA
	LTE-FDD B30 CH9820 @ 22.3 dBm	601	mA
	LTE-FDD B66 CH66786 @ 23.5 dBm	560	mA

Table 49: EG065K-EA Power Consumption

Description	Condition	Typ.	Unit
OFF State	Power off	24	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.32	mA
	LTE-FDD @ DRX = 0.32 s	4.32	mA
	LTE-FDD @ DRX = 0.64 s	3.10	mA
	LTE-FDD @ DRX = 0.64 s (USB suspended)	3.34	mA
	LTE-FDD @ DRX = 1.28 s	2.43	mA
	LTE-FDD @ DRX = 2.56 s	2.08	mA
	LTE-TDD @ DRX = 0.32 s	4.35	mA
	LTE-TDD @ DRX = 0.64 s	3.06	mA
	LTE-TDD @ DRX = 0.64 s (USB suspended)	3.35	mA
	LTE-TDD @ DRX = 1.28 s	2.36	mA
	LTE-TDD @ DRX = 2.56 s	2.04	mA
	WCDMA	TBD	mA
Idle state	LTE-FDD @ DRX = 0.64 s	11.92	mA
	LTE-FDD @ DRX = 0.64 s (USB active)	18.58	mA
	LTE-TDD @ DRX = 0.64 s	11.73	mA
	LTE-TDD @ DRX = 0.64 s, USB Active	18.63	mA
	WCDMA	TBD	mA
WCDMA data transfer	WCDMA B1	TBD	mA
	WCDMA B2	TBD	mA
	WCDMA B3	TBD	mA
	WCDMA B4	TBD	mA
	WCDMA B5	TBD	mA
	WCDMA B8	TBD	mA
LTE data transfer	LTE-FDD B1 CH300 @ 23.5 dBm	655	mA
	LTE-FDD B2 CH900 @ 23.5 dBm	610	mA
	LTE-FDD B3 CH1575 @ 23.5 dBm	620	mA

	LTE-FDD B4 CH2175 @ 23.5 dBm	595	mA
	LTE-FDD B5 CH2525 @ 23.5 dBm	620	mA
	LTE-FDD B7 CH3100 @ 23.5 dBm	710	mA
	LTE-FDD B8 CH3625 @ 23.5 dBm	650	mA
	LTE-FDD B20 CH6300 @ 23.5 dBm	650	mA
	LTE-FDD B28 CH9435 @ 23.5 dBm	650	mA
	LTE-TDD B40 CH39150 @ 23.5 dBm	390	mA

6.4. Digital I/O Characteristics

Table 50: VDD I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × VDD_EXT	VDD_EXT + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.3 × VDD_EXT	V
V_{OH}	High-level output voltage	VDD_EXT - 0.45	VDD_EXT	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 51: (U)SIM Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 52: (U)SIM High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, it is imperative to apply proper ESD countermeasures and handling methods. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 53: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interface	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 54: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-30	+25	+75	°C
Extended Temperature Range [5]	-40	-	+85	°C
Storage temperature range	-40	-	+90	°C

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

[4] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[5] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this extended temperature range, the module remains the ability to establish and maintain functions such as voice*, SMS, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are impervious, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

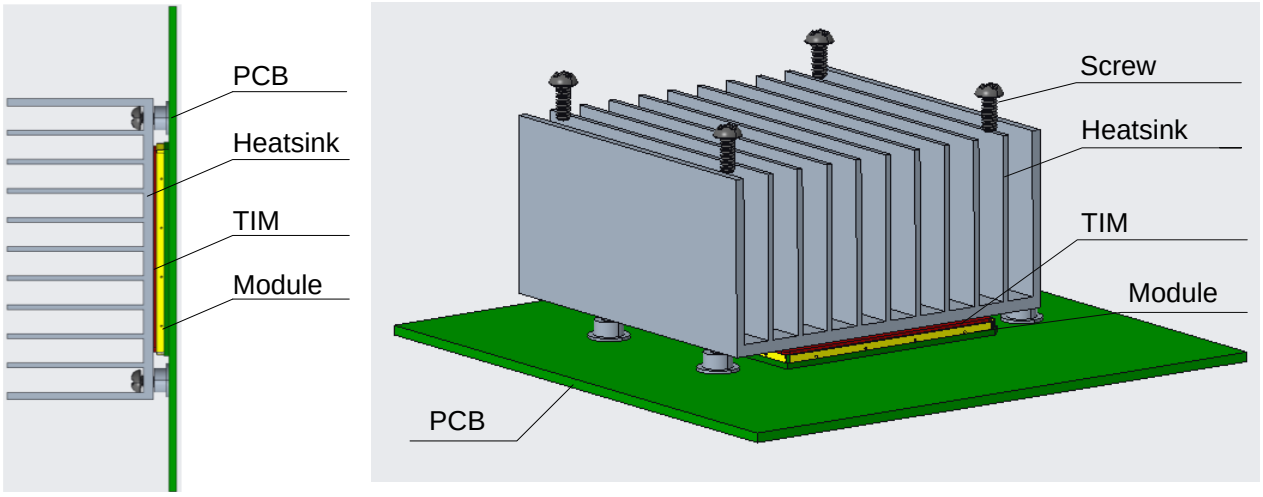


Figure 40: Placement and Fixing of Heatsink

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

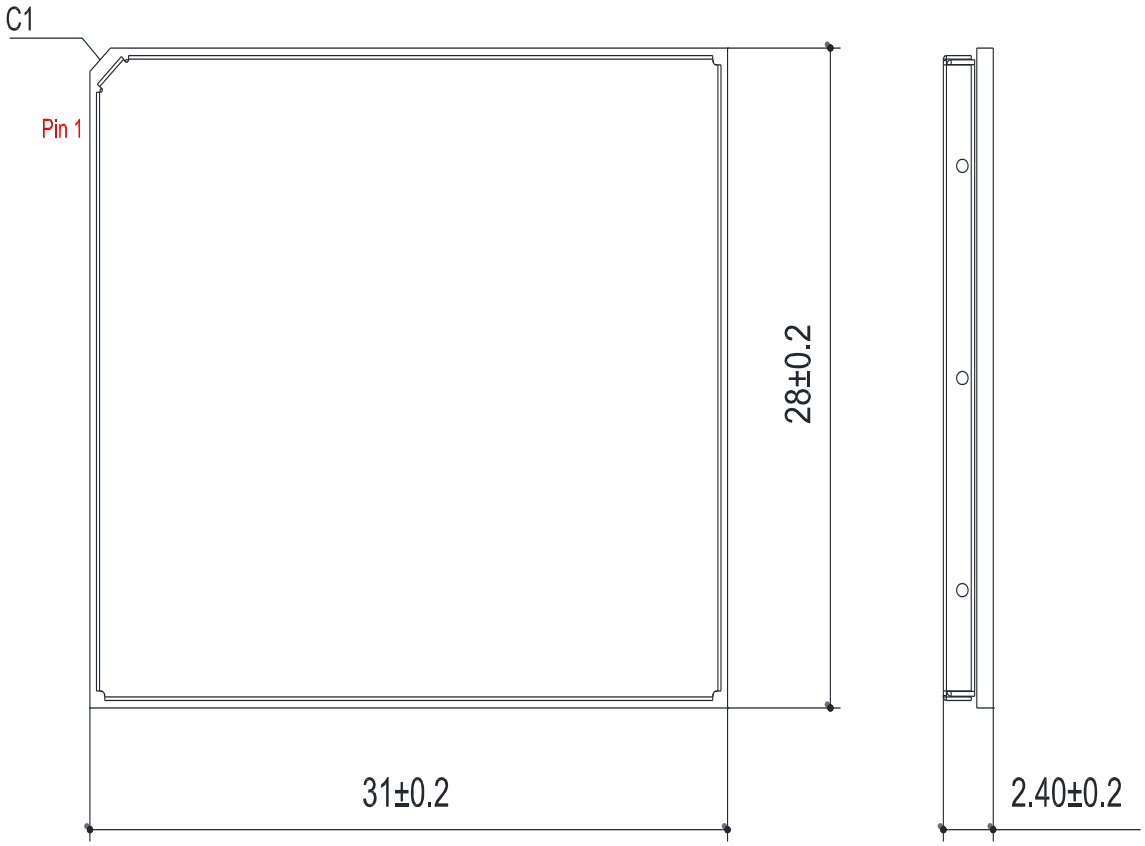


Figure 41: Module Top and Side Dimensions

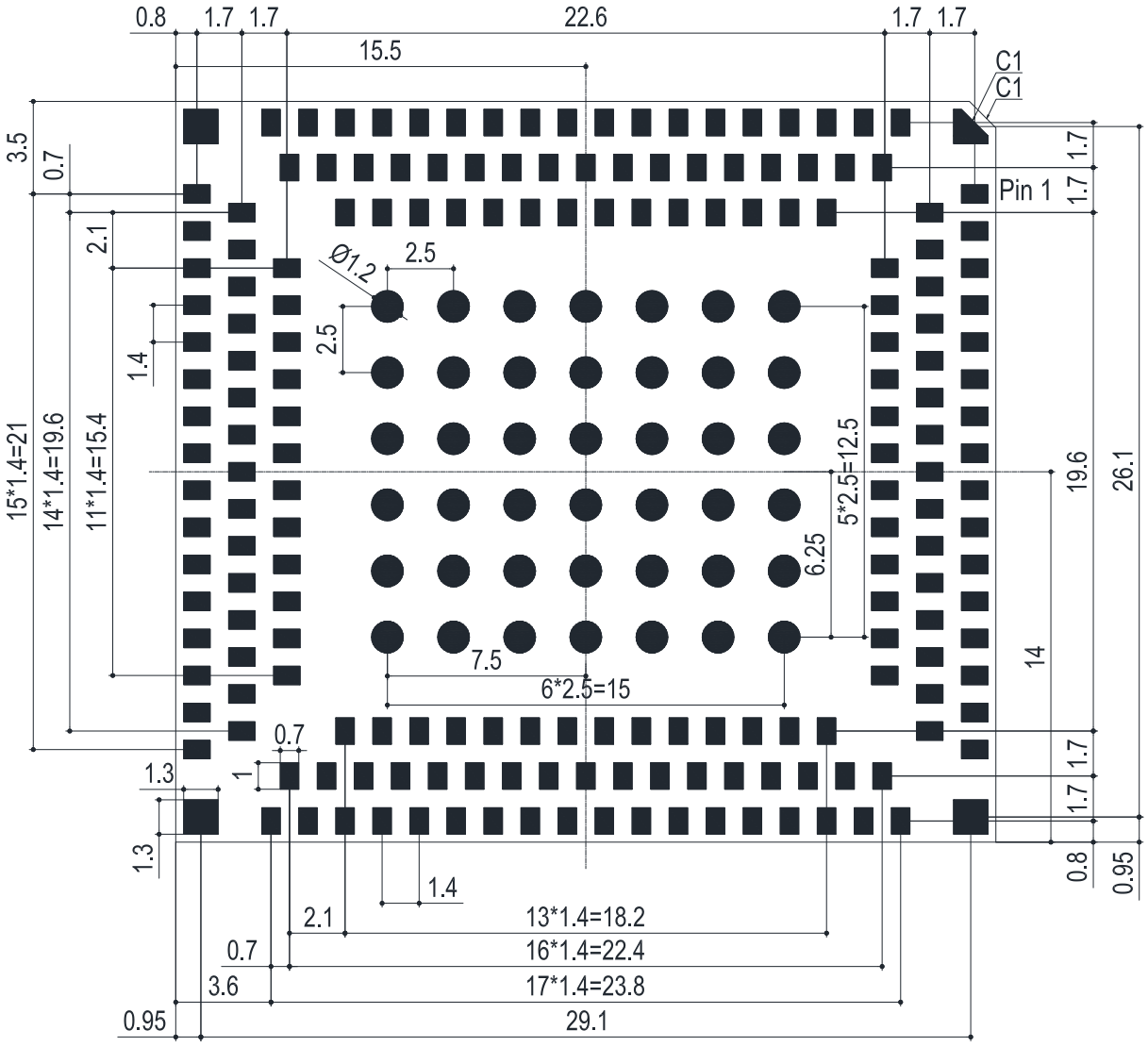


Figure 42: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

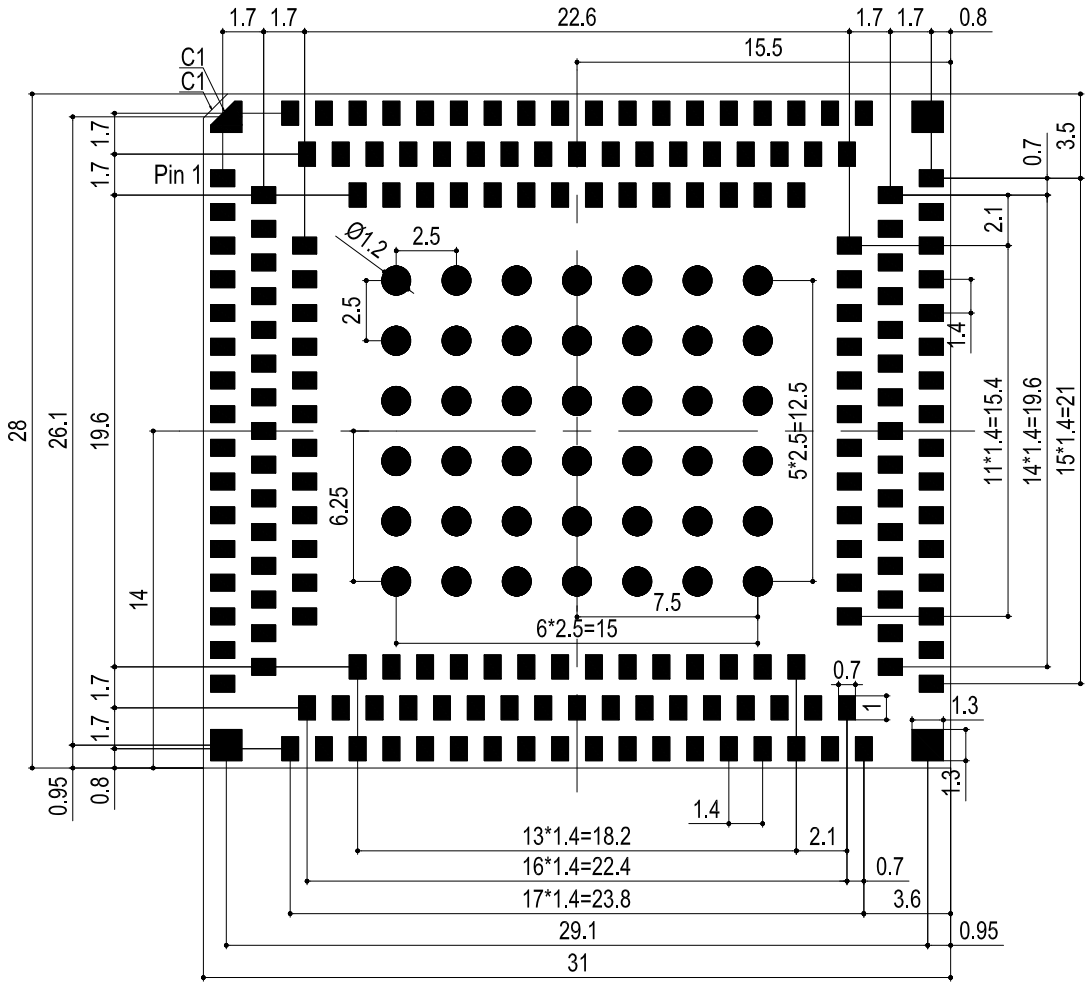


Figure 43: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

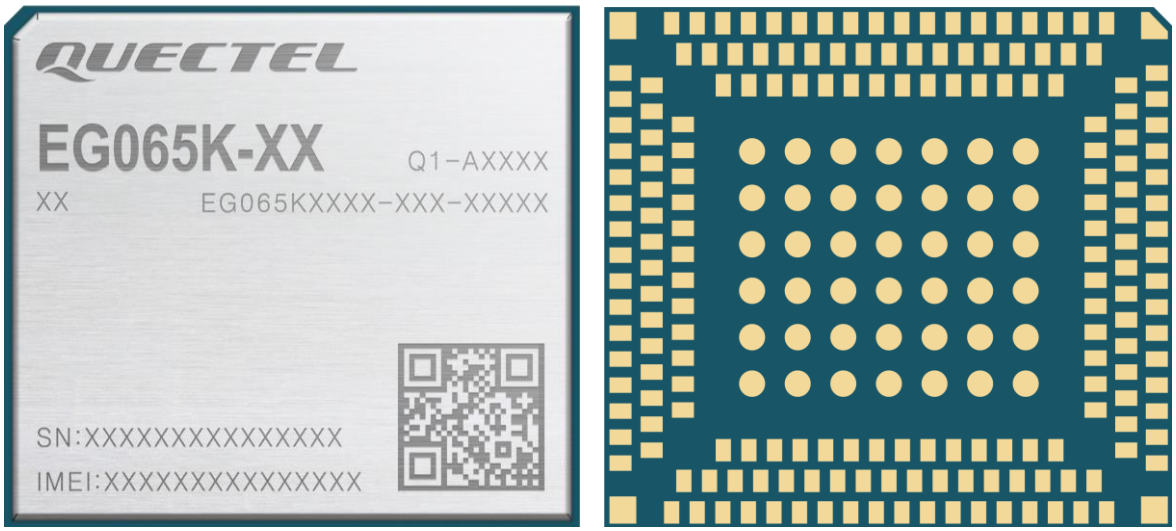


Figure 44: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [4]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

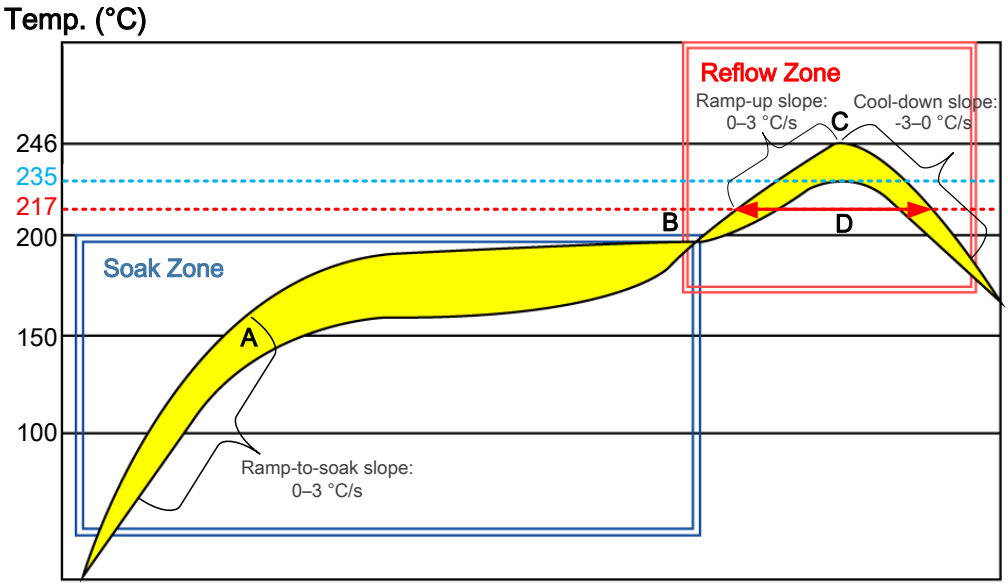


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 55: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

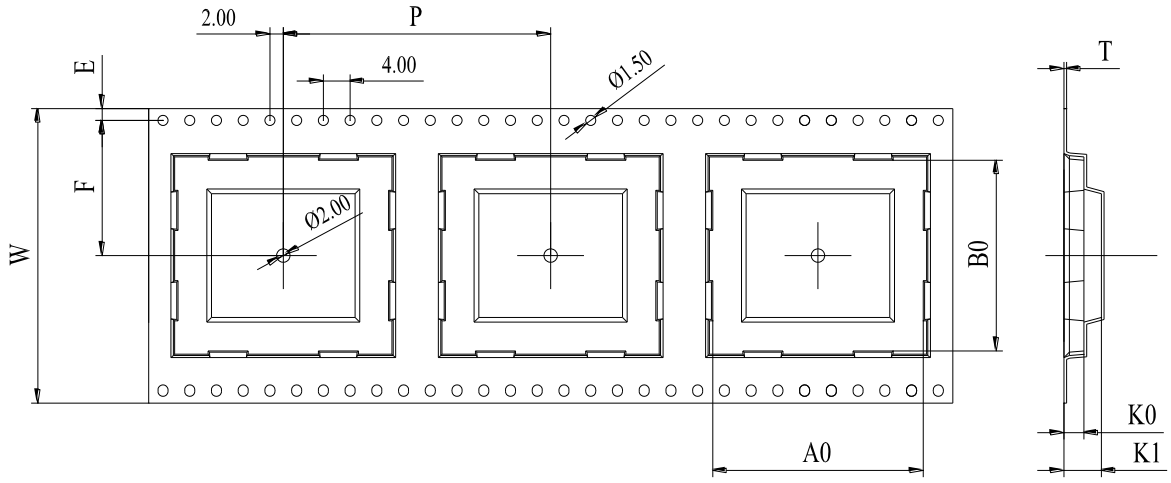


Figure 46: Carrier Tape Dimension Drawing

Table 56: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	40	0.4	31.5	28.5	3	5.6	20.2	1.75

8.3.2. Plastic Reel

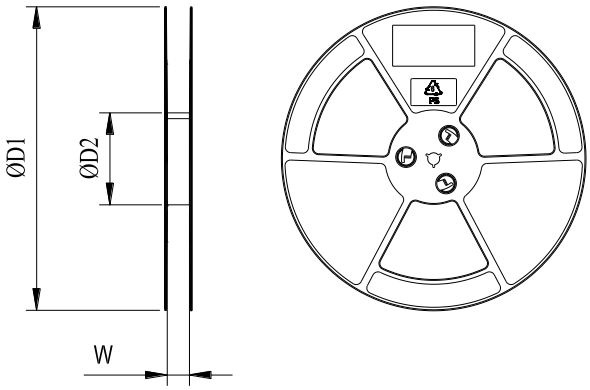


Figure 47: Plastic Reel Dimension Drawing

Table 57: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

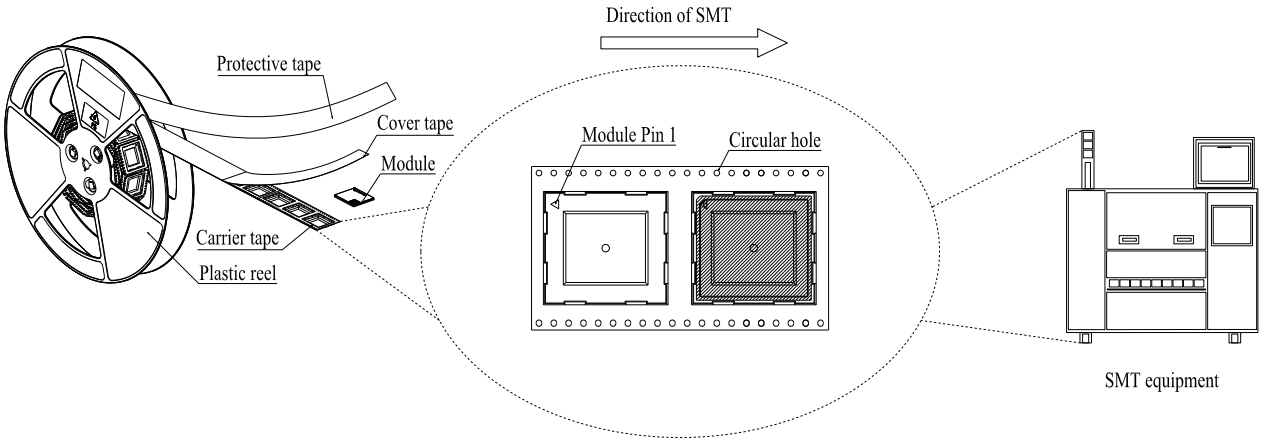
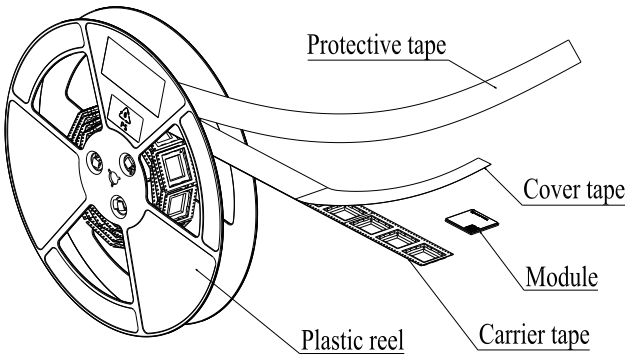


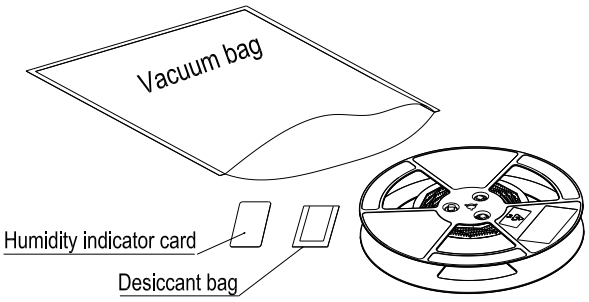
Figure 48: Mounting Direction

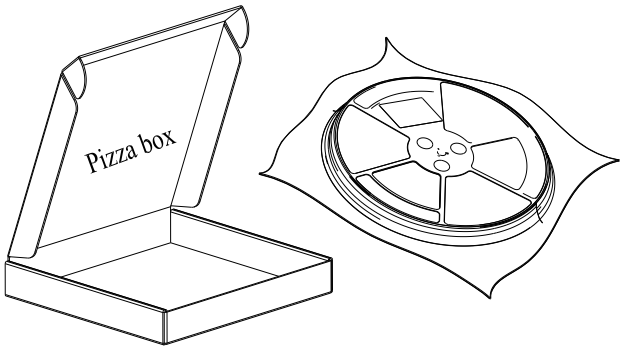
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

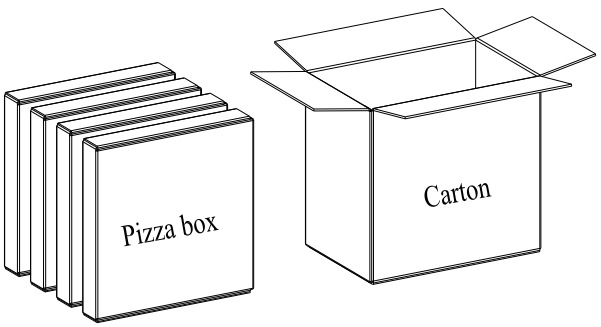


Figure 49: Packaging Process

9 Appendix References

Table 58: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EG06xK&Ex120K&EM060K_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_Application_Note

Table 59: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
bps	bit(s) per second
CHAP	Challenge-Handshake Authentication Protocol
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DRX	Discontinuous Reception/Diversity Receive
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FTP	File Transfer Protocol
GRFC	General RF Control
HB	High Band

HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Application Protocol Secured
IC	Integrated Circuit
I/O	Input/Output
LB	Low Band
LGA	Land Grid Array
LTE	Long Term Evolution
LwM2M	Lightweight M2M
MB	Middle Band
MBIM	Mobile Broadband Interface Model
MCU	Microcontroller Unit
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
M2M	Machine to Machine
NITZ	Network Identity and Time Zone
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation

QMI	Qualcomm Message Interface
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
Rx	Receive
SCS	Sub-Carrier Space
SD	Secure Digital
SMD	Surface Mount Device
SMS	Short Message Service
TDD	Time Division Duplex
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{OH}max	Maximum High-level Output Voltage

V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network