BG95xA&BG9x Series

Compatible Design

LPWA Module Series

Version: 1.0

Date: 2022-03-18

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Copyright © Quectel Wireless Solutions Co., Ltd. 2022. All rights reserved.

About the Document

Revision History

Version	Date	Author	Description
-	2021-12-02	Arvin WU/ Lex LI	Creation of the document
1.0	2022-03-18	Arvin WU/ Lex LI	First official release

Contents

About the Document **3**
Contents **4**
Table Index **5**
Figure Index **6**

1 Introduction **7**
1.1. Special Mark 7

2 General Description **8**
2.1. Product Description 8
2.2. Features Overview 12

3 Pin Definition **17**
3.1. Pin Assignment 18
3.2. Pin Comparison 20

4 Application Interfaces **25**
4.1. Power Supply 25
4.1.1. Reference Design for Power Supply 25
4.1.2. Voltage Stability Requirements 26
4.2. Turn On 28
4.3. Turn Off 33
4.3.1. Turn Off with PWRKEY 33
4.3.2. Turn Off with AT Command 34
4.4. Reset 35
4.5. PON_TRIG 37
4.6. (U)SIM Interface 38
4.7. UART Interfaces 40
4.8. USB Interface 42
4.9. PCM and I2C Interfaces 44
4.10. ADC Interfaces 44
4.11. GPIO Interfaces 45
4.12. GRFC Interface 46
4.13. RF Antenna Interfaces 46
4.14. Compatible Design Notices 48

5 Recommended Footprint **50**
5.1. Recommended Compatible Footprint 50
5.2. Installation Sketch Map 52

6 Appendix References **53**

Table Index

Table 1: Special Mark 7
Table 2: General Information 9
Table 3: Frequency Bands and GNSS Types 9
Table 4: Features Overview 12
Table 5: Definition of I/O Parameters 17
Table 6: Pin Comparison 20
Table 7: Reset Timing 36
Table 8: Data Rate and Function of USB Interface 42
Table 9: Related Documents 53
Table 10: Terms and Abbreviations 53

Figure Index

Figure 1: Pin Assignment (BG950A-GL/BG951A-GL/BG95 Series/BG96) 18
Figure 2: Reference Design of External Power Supply 26
Figure 3: Power Supply in Star-Shaped Pattern (BG950A-GL/BG951A-GL) 27
Figure 4: Power Supply in Star-Shaped Pattern (BG95 Series) 27
Figure 5: Power Supply in Star-Shaped Pattern (BG96) 28
Figure 6: Turn On the Module with a Driving Circuit 29
Figure 7: Turn On the Module with Button 29
Figure 8: Power-up Timing When VBAT is Stable for 100–200 ms (BG95xA-GL) 30
Figure 9: Power-up Timing When VBAT is Stable for More than 250 ms (BG95xA-GL) 30
Figure 10: Restart Timing (BG95xA-GL) 31
Figure 11: Power-up Timing (BG95 Series) 32
Figure 12: Power-up Timing (BG96) 32
Figure 13: Power-down Timing with PWRKEY & PON_TRIG (BG950A-GL/BG951A-GL) 33
Figure 14: Power-down Timing with PWRKEY (BG95 Series and BG96) 34
Figure 15: Power-down Timing with AT Command & PON_TRIG (BG950A-GL & BG951A-GL) 34
Figure 16: Power-down Timing with AT Command (BG95 Series/BG96) 35
Figure 17: Reference Design of RESET_N with a Driving Circuit 35
Figure 18: Reference Design of RESET_N with Button 36
Figure 19: Reset Timing 36
Figure 20: Reference Design of PON_TRIG (BG95 Series) 37
Figure 21: PON_TRIG Reference Design 1 (BG950A-GL/BG951A-GL) 37
Figure 22: PON_TRIG Reference Design 2 (BG950A-GL/BG951A-GL) 38
Figure 23: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector 39
Figure 24: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector 39
Figure 25: Reference Design with Translator Chip 41
Figure 26: Reference Design with Transistor Circuit 42
Figure 27: Reference Design of USB Interface (BG950A-GL/BG951A-GL/BG95 Series) 43
Figure 28: Reference Design of USB Interface (BG96) 43
Figure 29: Reference Design of PCM Application with Audio Codec (BG95 Series & BG96) 44
Figure 30: Reference Design of Main Antenna Interface 46
Figure 31: Reference Design of ANT_GNSS Interface (BG950A-GL & BG951A-GL) 47
Figure 32: Reference Design of GNSS Antenna Interface (BG95 Series & BG96) 47
Figure 33: Bottom Views of BG950A-GL/BG951A-GL/BG95 Series/BG96 50
Figure 34: Recommended Compatible Footprint (Top View) 51
Figure 35: Installation Sketch Map of BG950A-GL/BG951A-GL/BG95 Series/BG96 52

1 Introduction

Quectel BG95xA-GL modules are compatible with Quectel BG9x modules (LTE Cat M1, Cat NB1/Cat NB2 and EGPRS). This document briefly describes the compatible design between BG95xA-GL and BG9x modules.

In this document, BG95xA-GL includes BG950A-GL and BG951A-GL variants (LTE Cat M1, Cat NB1 and Cat NB2*), and BG9x includes BG95 series (LTE Cat M1, Cat NB2 and EGPRS) and BG96 (LTE Cat M1, Cat NB1 and EGPRS).

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 General Description

2.1. Product Description

BG950A-GL/BG951A-GL is an embedded IoT (LTE Cat M1, Cat NB1/NB2* [1]) wireless communication module. It provides data connectivity on LTE HD-FDD network, and supports half-duplex operation in LTE network. It also provides GNSS functionality to meet your specific application demands. For more details, see ***document [1]***.

BG95 is a series of embedded IoT (LTE Cat M1, LTE Cat NB2 [1] and EGPRS) wireless communication modules. It provides data connectivity on LTE HD-FDD and GPRS/EGPRS networks, and supports half-duplex operation in LTE network. It also provides GNSS and voice* functionality [2] to meet your specific application demands. For more details, see ***document [2]***.

BG96 is an embedded IoT (LTE Cat M1, LTE Cat NB1 and EGPRS) wireless communication module. It provides data connectivity on LTE HD-FDD and GPRS/EGPRS networks, and supports half-duplex operation in LTE network. It also provides GNSS [3] and voice functionality [2] to meet your specific application demands. For more details, see ***document [3]***.

BG950A-GL/BG951A-GL, BG95 series and BG96 modules are designed as compatible products. You can choose a suitable module according to specific application requirements. The compatible design guideline ensures a smooth migration for your products between the modules.

[1] LTE Cat NB2 is backward compatible with LTE Cat NB1.
[2] BG95 series and BG96 support VoLTE (Voice over LTE) under LTE Cat M1. Additionally, BG95-M3 and BG95-M5 support CS voice under GSM. BG950A-GL/BG951A-GL do not support VoLTE function.
[3] GNSS function is optional on BG96.

Table 2: General Information

Module	Appearance	Packaging	Dimensions (mm)	Description
BG950A-GL		102 LGA pins	23.6 × 19.9 × 2.2	LTE Cat M1/Cat NB1/ Cat NB2* module
BG951A-GL		102 LGA pins	23.6 × 19.9 × 2.2	LTE Cat M1/Cat NB1/ Cat NB2* module
BG95 series		102 LGA pins	23.6 × 19.9 × 2.2	LTE Cat M1/Cat NB2/ EGPRS module
BG96		102 LGA pins	26.5 × 22.5 × 2.3	LTE Cat M1/Cat NB1/ EGPRS module

Table 3: Frequency Bands and GNSS Types

Module	Supported Bands	LTE Bands Power Class	GNSS [3]
BG950A-GL	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B66 **Cat NB1/NB2*:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/ B19/B20/B25/B28/B66	Power Class 3 (23 dBm ± 2.7 dB)	GPS, GLONASS
BG951A-GL	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/	Power Class 3 (23 dBm ± 2.7 dB)	GPS, GLONASS, BDS, Galileo,

	B20/B25/B26/B27/B28/B66 **Cat NB1/NB2*:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/ B19/B20/B25/B28/B66		QZSS
BG95-M1	**Cat M1 Only:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B66/B85	Power Class 5 (21 dBm)	GPS, GLONASS, BDS, Galileo, QZSS
BG95-M2	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B66/B85 **Cat NB2:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B28/B66/B71/B85	Power Class 5 (21 dBm)	GPS, GLONASS, BDS, Galileo, QZSS
BG95-M3	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B66/B85 **Cat NB2:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B28/B66/B71/B85 **EGPRS:** 850/900/1800/1900 MHz	Power Class 5 (21 dBm)	GPS, GLONASS, BDS, Galileo, QZSS
BG95-M4	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B31/B66/B72/ B73/B85 **Cat NB2:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B28/B31/B66/B72/B73/B85	Power Class 2 (26 dBm) [4] @ B31/B72/B73 Power Class 3 (23 dBm) [4] @ B31/B72/B73 Power Class 5 (21 dBm) @ other LTE bands	GPS, GLONASS, BDS, Galileo, QZSS
BG95-M5	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B66/B85 **Cat NB2:**	Power Class 3 (23 dBm)	GPS, GLONASS, BDS, Galileo, QZSS

[4] LTE HD-FDD B31, B72 and B73 on BG95-M4 support either Power Class 2 (26 dBm) or Power Class 3 (23 dBm). For more details, consult Quectel Technical Support (support@quectel.com).

	LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B28/B66/B71/B85 **EGPRS:** 850/900/1800/1900 MHz		
BG95-M6	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B66/B85 **Cat NB2:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B28/B66/B71/B85	Power Class 3 (23 dBm)	GPS, GLONASS, BDS, Galileo, QZSS
BG95-MF	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B27/B28/B66/B85 **Cat NB2:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B28/B66/B71/B85 **Wi-Fi (For positioning only):** 2.4 GHz	Power Class 5 (21 dBm)	GPS, GLONASS, BDS, Galileo, QZSS
BG96	**Cat M1 & Cat NB1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25 [5]/B26*/B28 **EGPRS:** 850/900/1800/1900 MHz	Power Class 3 (23 dBm)	GPS, GLONASS, BDS, Galileo, QZSS

[5] LTE B25 is supported on BG96 with R1.2 hardware version.

2.2. Features Overview

The general features of BG950A-GL, BG951A-GL, BG95 series and BG96 modules are compared in the table below.

Table 4: Features Overview

Feature	BG950A-GL/BG951A-GL	BG95 Series	BG96
Power Supply	Supply voltage [6]: 2.2–4.35 V, Typ. 3.3 V	**BG95-M1/-M2/:** Supply voltage [7]: 2.6–4.8 V, Typ. 3.3 V **BG95-M3/-M5/-M6/-MF:** Supply voltage: 3.3–4.3 V, Typ. 3.8 V **BG95-M4:** Supply voltage: 3.2–4.2 V, Typ. 3.8 V	Supply voltage: 3.3–4.3 V, Typ. 3.8 V
Peak Current	**VBAT_BB:** Max. 0.2 A **VBAT_RF:** Max. 1.5 A	**VBAT_BB:** Max. 0.6 A **VBAT_RF:** Max. 2.7 A	**VBAT_BB:** Max. 0.5 A **VBAT_RF:** Max. 2.0 A
PSM Current	Avg. 1.5 μA @ BG950A-GL & BG951A-GL	Avg. 4 μA @ BG95-M1 Avg. 3.89 μA @ BG95-M2 Avg. 3.89 μA @ BG95-M3 Avg. 3.94 μA @ BG95-M4 Avg. 5.10 μA @ BG95-M5 Avg. 4.32 μA @ BG95-M6	Avg. 10 μA

[6] When the module starts up normally, in order to ensure full-function mode, the minimum power supply voltage should be higher than 2.2 V. For every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. In order to ensure that the module can start normally, pull down PWRKEY to turn on the module after VBAT remains stable for 100 ms.
[7] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.

		Avg. 4.04 μA @ BG95-MF	
Sleep Current	**LTE Cat M1 @ DRX = 1.28 s:** 1.1 mA @ BG950A-GL & BG951A-GL **LTE Cat NB1 @ DRX = 1.28 s:** 2.2 mA @ BG950A-GL & BG951A-GL	**LTE Cat M1 @ DRX = 1.28 s:** 1.7 mA @ BG95-M1 1.68 mA @ BG95-M2 1.89 mA @ BG95-M3 1.53 mA @ BG95-M4 1.56 mA @ BG95-M5 1.42 mA @ BG95-M6 1.59 mA @ BG95-MF **LTE Cat NB1 @ DRX = 1.28 s:** 1.55 mA @ BG95-M2 1.49 mA @ BG95-M3 1.39 mA @ BG95-M4 1.43 mA @ BG95-M5 1.31 mA @ BG95-M6 1.43 mA @ BG95-MF	**LTE Cat M1 @ DRX = 1.28 s:** 1.54 mA **LTE Cat NB1 @ DRX = 1.28 s:** 2.03 mA
LTE Features	● Support 3GPP Rel-14* ● Supports LTE Cat M1 and LTE Cat NB1/NB2* ● Supports 1.4 MHz RF bandwidth for LTE Cat M1 ● Support 200 kHz RF bandwidth for LTE Cat NB1/NB2* ● Cat M1: 588 kbps (DL)/1119 kbps (UL) ● Cat NB1: 27.2 kbps (DL)/62.5 kbps (UL) ● Cat NB2*:	● Supports 3GPP Rel-14 ● Supports LTE Cat M1 and LTE Cat NB2 ● Supports 1.4 MHz RF bandwidth for LTE Cat M1 ● Supports 200 kHz RF bandwidth for LTE Cat NB2 ● Cat M1: Max. 588 kbps (DL)/1119 kbps (UL) ● Cat NB2: Max. 127 kbps (DL)/158.5 kbps (UL)	● Supports LTE Cat M1 and LTE Cat NB1 ● Supports 1.4 MHz RF bandwidth for LTE Cat M1 ● Supports 200 kHz RF bandwidth for LTE Cat NB1 ● Supports SISO in DL direction ● Cat M1: Max. 375 kbps (DL)/375 kbps (UL) ● Cat NB1: Max. 32 kbps (DL)/70 kbps (UL)

	127 kbps (DL)/158 kbps (UL)		
Temperature Range	Operating temperature range: -35 to +75 °C [8] Extended temperature range: -40 to +85 °C [9] Storage temperature range: -40 to +90 °C	Operating temperature range: -35 to +75 °C [8] Extended temperature range: -40 to +85 °C [9] Storage temperature range: -40 to +90 °C	Operating temperature range: -35 to +75 °C [8] Extended temperature range: -40 to +85 °C [9] Storage temperature range: -40 to +90 °C
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps baud by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **CLI UART:** ● Used for firmware upgrade, software debugging, log output, GNSS data and NMEA sentences output ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow	**Main UART:** ● Used for data transmission and AT command communication ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for software debugging and log output ● 115200 bps baud rate **GNSS UART:** ● Used for GNSS data and NMEA sentences output ● 115200 bps baud rate by default	**UART1:** ● Used for data transmission and AT command communication ● 115200 bps by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **UART2:** ● Used for module debugging and log output ● 115200 bps baud rate **UART3:** ● Used for outputting GNSS data or NMEA sentences ● 115200 bps baud rate

[8] Within the operating temperature range, the module meets 3GPP specifications.
[9] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call (BG950A-GL, BG951A-GL and BG95 series do not support emergency call, the voice and SMS function of BG950A-GL and BG951A-GL are under development.), without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

	control **Debug UART:** ● Used for RF calibration and log output ● 961200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **CLI/GNSS UART:** ● Used for GNSS data and NMEA sentences output and GNSS firmware upgrade ● 115200 bps baud rate by default		
USB Interface [10]	● USB 2.0 (slave only) ● Supports full speed (12 Mbps) only	● USB 2.0 (slave only) ● Supports high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps)	● USB 2.0 (slave only) ● Supports high speed (480 Mbps) and full speed (12 Mbps)
Digital Audio	Not Supported	Dedicated PCM interface* for VoLTE or GSM CS voice	PCM interface
I2C Interface	Not Supported	Under development (dedicated for VoLTE or GSM CS voice)	Supported
ADC	Two ADCs	Two ADCs [11]	Two ADCs
(U)SIM Card Detection	Supported	Supported	Supported

[10] For BG950A-GL and BG951A-GL, USB interface is under development.
[11] BG95 series supports ADC0 and ADC1. ADC1 connects directly to ADC0 inside the module, therefore they cannot be used simultaneously. If the two ADC interfaces are intended to be used at the same time, please add an external analog switch.

Firmware Upgrade	• CLI UART interface • USB 2.0 interface* • DFOTA	• USB 2.0 interface • DFOTA	• USB 2.0 interface • DFOTA

3 Pin Definition

The I/O parameter definition of BG950A-GL, BG951A-GL, BG95 series and BG96 modules is presented in the table below.

Table 5: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

3.1. Pin Assignment

The following figure shows the pin assignment of BG950A-GL, BG951A-GL, BG95 series and BG96.

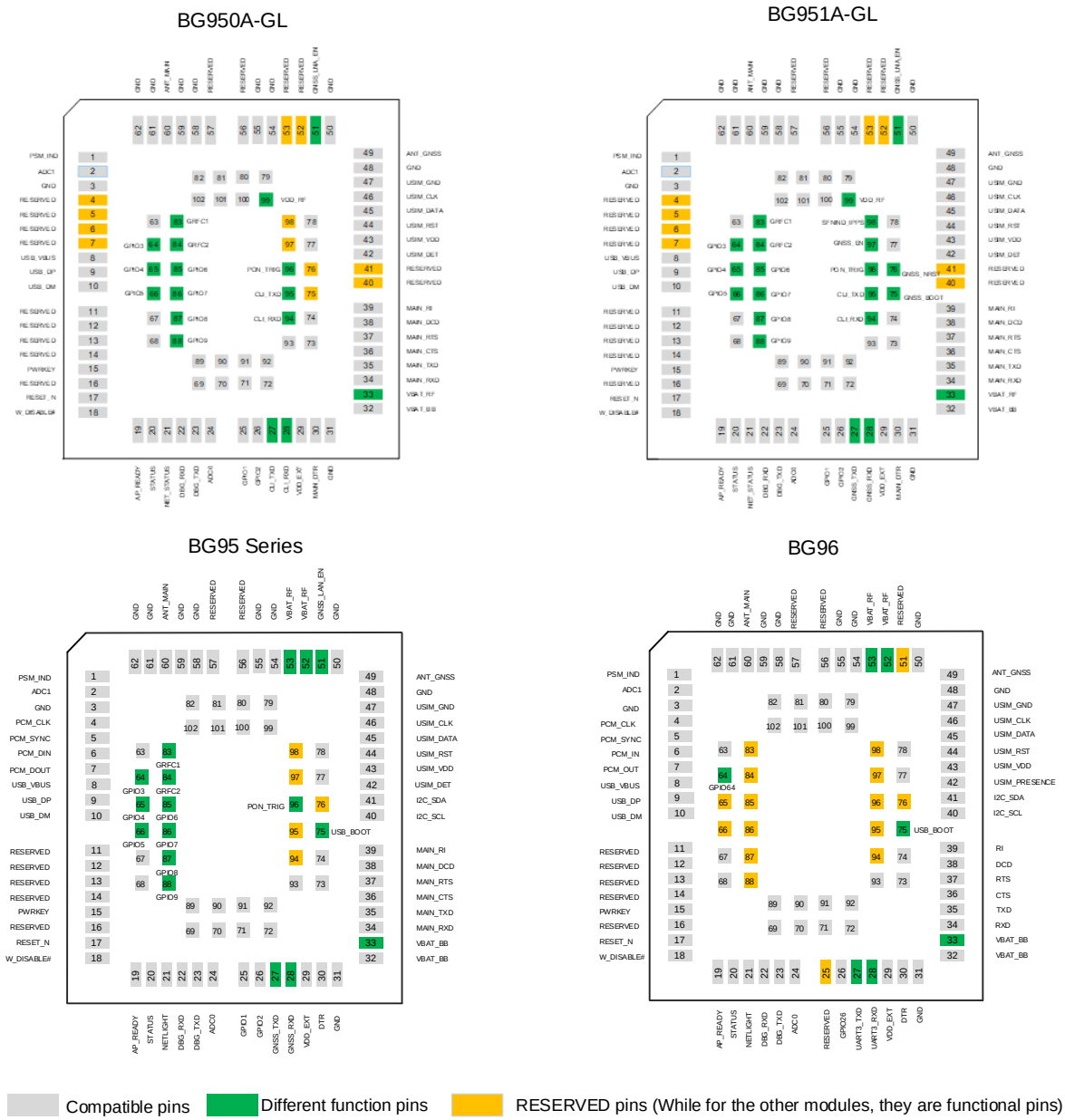


Figure 1: Pin Assignment (BG950A-GL/BG951A-GL/BG95 Series/BG96)

NOTE

1. On BG950A-GL/BG951A-GL/BG95 series/BG96, ADC input voltage must not exceed 1.8 V.
2. **For BG950A-GL and BG951A-GL:**
   1) On BG950A-GL/BG951A-GL, PWRKEY is pulled up to an internal voltage of the baseband chipset inside the module, and the minimum high-level output voltage is 1.0 V.
   2) BG950A-GL/BG951A-GL integrates an LNA, therefore it is not recommended to use an external LNA. It is strongly recommended to keep GNSS_LNA_EN (pin 51) and VDD_RF (pin 99) unconnected.
   3) On BG950A-GL, pin 27 and pin 28 only function as CLI UART interface (pin 27: CLI_TXD; pin 28: CLI_RXD). In this case, the two pins are connected to pin 95 and pin 94 respectively inside the module.
   4) On BG951A-GL, pin 27 and pin 28 only function as GNSS UART interface (pin 27: GNSS_TXD; pin 28: GNSS_RXD).
   5) Only BG951A-GL supports GNSS_BOOT (pin 75), GNSS_NRST (pin 76), GNSS_EN (pin 97), and SFNIND_1PPS (pin 98).
   6) BG950A-GL/BG951A-GL can be reset by driving RESET_N low for at least 100 ms and releasing it.
   7) BG950A-GL/BG951A-GL does not support PCM and I2C interfaces.
3. **For BG95 series:**
   1) PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
   2) Supports ADC0 and ADC1. The two interfaces are internally connected, therefore they cannot be used simultaneously. If the two ADC interfaces are intended to be used at the same time, please add an external analog switch.
   3) GNSS_TXD (pin 27), GRFC2 (pin 84) and GNSS_LNA_EN (pin 51) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
   4) Only BG95-MF supports ANT_WIFI (pin 56). Only BG95-M4/-MF supports GNSS_LNA_EN (pin 51).
   5) BG95-MF does not support GPIO3 and GPIO4 interfaces (pin 64 and pin 65).
   6) BG95-M4 does not support GRFC interfaces (pin 83 and pin 84).
   7) GPIO1 (pin 25) supports fast shutdown function. This function is disabled by default. See ***document [2]*** for more details.
   8) BG95 series can be reset by driving RESET_N low for 2–3.8 s and releasing it. RESET_N connects directly to PWRKEY inside the module.
   9) PCM and I2C interfaces are used for VoLTE or GSM CS voice only.
4. **For BG96:**
   1) PWRKEY output voltage is 0.8 V because of the diode drop inside the chipset.
   2) BG96 can be reset by driving RESET_N low for 150–460 ms and releasing it.
   3) PCM and I2C interfaces are used for VoLTE only.

3.2. Pin Comparison

Table 6: Pin Comparison

Pin No.	BG950A-GL/BG951A-GL				BG95 Series				BG96			
	Pin Name	I/O	Power Domain	Description	Pin Name	I/O	Power Domain	Description	Pin Name	I/O	Power Domain	Description
1	PSM_IND [12]	DO	1.8 V	Indicate the module's power saving mode	PSM_IND [12]	DO	1.8 V	Indicate the module's power saving mode	PSM_IND [12]	DO	1.8 V	Indicate the module's power saving mode
2	ADC1	AI	0–1.8 V	General-purpose ADC interface	ADC1 [13]	AI	0.1–1.8 V	General-purpose ADC interface	ADC1	AI	0.3–1.8 V	General-purpose ADC interface
3	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
4	RESERVED	-	-	Reserved	PCM_CLK*	DO	1.8 V	PCM clock output	PCM_CLK	DO	1.8 V	PCM clock output
5	RESERVED	-	-	Reserved	PCM_SYNC*	DO	1.8 V	PCM data frame sync	PCM_SYNC	DO	1.8 V	PCM data frame sync
6	RESERVED	-	-	Reserved	PCM_DIN*	DIO	1.8 V	PCM data input	PCM_IN	DIO	1.8 V	PCM data input.
7	RESERVED	-	-	Reserved	PCM_DOUT*	DIO	1.8 V	PCM data output	PCM_OUT	DIO	1.8 V	PCM data output.
8	USB_VBUS*	AI	Typ. 5.0 V	USB connection detect	USB_VBUS	AI	Typ. 5.0 V	USB connection detect	USB_VBUS	AI	Typ. 5.0 V	USB connection detect
9	USB_DP*	AIO	-	USB differential data (+)	USB_DP	AIO	-	USB differential data (+)	USB_DP	AIO	-	USB differential data (+)
10	USB_DM*	AIO	-	USB differential data (-)	USB_DM	AIO	-	USB differential data (-)	USB_DM	AIO	-	USB differential data (-)
11–14	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
15	PWRKEY [14]	DI	-	Turn on/off the module	PWRKEY [15]	DI	-	Turn on/off the module	PWRKEY [16]	DI	0.8 V	Turn on/off the module
16	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
17	RESET_N [17]	DI	-	Reset the module	RESET_N [17]	DI	1.5 V	Reset the module	RESET_N [17]	DI	1.8 V	Reset the module
18	W_DISABLE#	DI	1.8 V	Airplane mode control	W_DISABLE#	DI	1.8 V	Airplane mode control	W_DISABLE#	DI	1.8 V	Airplane mode control
19	AP_READY*	DI	1.8 V	Application processor sleep state detect	AP_READY	DI	1.8 V	Application processor sleep state detect	AP_READY	DI	1.8 V	Application processor sleep state detect

[12] When PSM is enabled, the function of PSM_IND pin will be activated after the module is rebooted. When PSM_IND is in high voltage level, the module is in normal operation state, and when it is in low voltage level, the module is in PSM.
[13] BG95 series supports ADC0 and ADC1. ADC1 connects directly to ADC0 inside the module, therefore they cannot be used simultaneously. If the two ADC interfaces are intended to be used at the same time, please add an external analog switch.
[14] On BG950A-GL and BG951A-GL, the minimum high-level output voltage of PWRKEY output is 1.0 V. PWRKEY is internally pulled up to an internal voltage in the baseband chipset, and its output voltage is the internal voltage minus a diode drop in the chipset.
[15] On BG95 series, PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
[16] On BG96, PWRKEY output voltage is 0.8 V because of the diode drop inside the chipset.
[17] BG950A-GL and BG951A-GL can be reset by driving RESET_N low for at least 100 ms. BG95 series can be reset by driving RESET_N low for 2–3.8 s. BG96 can be reset by driving RESET_N low for 150–460 ms.

20	STATUS	DO	1.8 V	Indicate the module's operation status	STATUS	DO	1.8 V	Indicate the module's operation status	STATUS	DO	1.8 V	Indicate the module's operation status
21	NET_STATUS	DO	1.8 V	Indicate the module's network activity status	NET_STATUS	DO	1.8 V	Indicate the module's network activity status.	NETLIGHT	DO	1.8 V	Indicate the module's network activity status
22	DBG_RXD	DI	1.8 V	Debug UART receive	DBG_RXD	DI	1.8 V	Debug UART receive	DBG_RXD	DI	1.8 V	Debug UART receive
23	DBG_TXD	DO	1.8 V	Debug UART transmit	DBG_TXD	DO	1.8 V	Debug UART transmit	DBG_TXD	DO	1.8 V	Debug UART transmit
24	ADC0	AI	0–1.8 V	General-purpose ADC interface	ADC0 [13]	AI	0.1–1.8 V	General-purpose ADC interface	ADC0	AI	0.3–1.8 V	General-purpose ADC interface
25	GPIO1	DIO	1.8 V	General-purpose input/output	GPIO1	DIO	1.8 V	General-purpose input/output	RESERVED	-	-	Reserved
26	GPIO2	DIO	1.8 V	General-purpose input/output	GPIO2	DIO	1.8 V	General-purpose input/output	GPIO26	DIO	1.8 V	General-purpose input and output
27	CLI/GNSS_TXD [18]	DO	1.8 V	Reserved/GNSS UART transmit	GNSS_TXD	DO	1.8 V	GNSS UART transmit	UART3_TXD	DO	1.8 V	UART3 transmit
28	CLI/GNSS_RXD [18]	DI	1.8 V	Reserved/GNSS UART receive	GNSS_RXD	DI	1.8 V	GNSS UART receive	UART3_RXD	DI	1.8 V	UART3 receive
29	VDD_EXT	PO	-	Provide 1.8 V for external circuits	VDD_EXT	PO	1.8 V	Provide 1.8 V for external circuits	VDD_EXT	PO	-	Provide 1.8 V for external circuits
30	MAIN_DTR	DI	1.8 V	Main UART data terminal ready	MAIN_DTR	DI	1.8 V	Main UART data terminal ready	DTR	DI	1.8 V	Main UART data terminal ready
31	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
32, 33	VBAT_BB	PI	Voltage range [19]: 2.2–4.35 V, typ. 3.3 V	Power supply for the module's baseband part	VBAT_BB	PI	**BG95-M1/-M2:** Voltage range [20]: 2.6–4.8 V, typ. 3.3 V **BG95-M3/-M5/-M6/-MF:** Voltage range: 3.3–4.3 V, typ. 3.8 V **BG95-M4:** Voltage range: 3.2–4.2 V, typ. 3.8 V	Power supply for module's baseband part	VBAT_BB	PI	Voltage range: 3.3–4.3 V, typ. 3.8 V	Power supply for the module's baseband part
	VBAT_RF	PI	2.2–4.35 V, typ. 3.3 V	Power supply for the module's RF part								
34	MAIN_RXD	DI	1.8 V	Main UART receive	MAIN_RXD	DI	1.8 V	Main UART receive	RXD	DI	1.8 V	Receive
35	MAIN_TXD	DO	1.8 V	Main UART transmit	MAIN_TXD	DO	1.8 V	Main UART transmit	TXD	DO	1.8 V	Transmit

[18] On BG950A-GL, pin 27 and pin 28 only function as CLI UART interface (pin 27: CLI_TXD; pin 28: CLI_RXD). In this case, the two pins are connected to pin 95 and pin 94 respectively inside the module. On BG951A-GL, pin 27 and pin 28 only function as GNSS UART interface (pin 27: GNSS_TXD; pin 28: GNSS_RXD).
[19] On BG950A-GL and BG951A-GL, every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. After the module starts up normally, in order to ensure full-function mode, the minimum power supply voltage should be higher than 2.2 V.
[20] On BG95 series, every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.

36	MAIN_CTS	DO	1.8 V	DTE clear to send signal from DCE (Connect to DTE's CTS)	MAIN_CTS	DO	1.8 V	DTE clear to send signal from DCE (Connect to DTE's CTS)	CTS	DO	1.8 V	DTE clear to send signal from DCE (Connect to DTE's CTS)
37	MAIN_RTS	DI	1.8 V	DTE request to send signal to DCE (Connect to DTE's RTS)	MAIN_RTS	DI	1.8 V	DTE request to send signal to DCE (Connect to DTE's RTS)	RTS	DI	1.8 V	DTE request to send signal to DCE (Connect to DTE's RTS)
38	MAIN_DCD	DO	1.8 V	Main UART data carrier detect	MAIN_DCD	DO	1.8 V	Main UART data carrier detect	DCD	DO	1.8 V	Data carrier detect
39	MAIN_RI*	DO	1.8 V	Main UART ring indication	MAIN_RI	DO	1.8 V	Main UART ring indication	RI	DO	1.8 V	Ring indication
40	RESERVED	-	-	Reserved	I2C_SCL*	OD	1.8 V only.	I2C serial clock (for external codec)	I2C_SCL	OD	1.8 V only	I2C serial clock (for external codec)
41	RESERVED	-	-	Reserved	I2C_SDA*	OD	1.8 V only.	I2C serial clock (for external codec)	I2C_SDA	OD	1.8 V only	I2C serial data (for external codec)
42	USIM_DET	DI	1.8 V	(U)SIM card hot-plug detect	USIM_DET	DI	1.8 V	(U)SIM card hot-plug detect	USIM_ PRESENCE	DI	1.8 V	(U)SIM card hot-plug detect
43	USIM_VDD	PO	1.8 V only	(U)SIM card power supply	USIM_VDD	PO	1.8 V	(U)SIM card power supply	USIM_VDD	PO	1.8/3.0 V	(U)SIM card power supply
44	USIM_RST	DO	1.8 V	(U)SIM card reset	USIM_RST	DO	1.8 V	(U)SIM card reset.	USIM_RST	DO	1.8/3.0 V	(U)SIM card reset.
45	USIM_DATA	DIO	1.8 V	(U)SIM card data	USIM_DATA	DIO	1.8 V	(U)SIM card data	USIM_DATA	DIO	1.8/3.0 V	(U)SIM card data
46	USIM_CLK	DO	1.8 V	(U)SIM card clock	USIM_CLK	DO	1.8 V	(U)SIM card clock	USIM_CLK	DO	1.8/3.0 V	(U)SIM card clock
47	USIM_GND	-	-	Specified ground for (U)SIM card	USIM_GND	-	-	Specified ground for (U)SIM card	USIM_GND	-	-	Specified ground for (U)SIM card
48	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
49	ANT_GNSS	AI	-	GNSS antenna interface	ANT_GNSS	AI	-	GNSS antenna interface	ANT_GNSS	AI	-	GNSS antenna interface
50	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
51	GNSS_LNA_ EN	DO	1.8 V	External GNSS LNA enable	GNSS_LNA_ EN [21]	DO	1.8 V	External GNSS LNA enable	RESERVED	-	-	Reserved
52–53	RESERVED	-	-	Reserved	VBAT_RF	PI	**BG95-M1/-M2/:** Voltage range [20]: 2.6–4.8 V, Typ. 3.3 V **BG95-M3/-M5/-M6/-MF:** 3.3–4.3 V, Typ. 3.8 V **BG95-M4:** 3.2–4.2 V Typ.	Power supply for the module's RF part	VBAT_RF	PI	Voltage range: 3.3–4.3 V, typ. 3.8 V	Power supply for the module's RF part

[21] Only BG95-M4/-MF supports GNSS_LNA_EN (pin 51).

						3.8 V						
54	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
55	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
56	RESERVED	-	-	Reserved	ANT_WIFI*	AI	-	Wi-Fi antenna interface for BG95-MF only.	RESERVED	-	-	Reserved
57	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
58	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
59	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
60	ANT_MAIN	AIO	-	Main antenna interface	ANT_MAIN	AIO	-	Main antenna interface	ANT_MAIN	AIO	-	Main antenna interface
61	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
62	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
63	RESERVED	-	-	-	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
64	GPIO3	DIO	1.8 V	General-purpose input/output	GPIO3	DIO	1.8 V	General-purpose input/output	GPIO64	DIO	1.8 V	General-purpose input/output
65	GPIO4	DIO	1.8 V	General-purpose input/output	GPIO4	DIO	1.8 V	General-purpose input/output	RESERVED	-	-	Reserved
66	GPIO5	DIO	1.8 V	General-purpose input/output	GPIO5	DIO	1.8 V	General-purpose input/output	RESERVED	-	-	Reserved
67–74	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
75	GNSS_BOOT	DI	1.8 V	Force the GNSS chip of the module into emergency download mode	USB_BOOT	DI	1.8 V	Force the module into emergency download mode	USB_BOOT	DI	1.8 V	Force the module into emergency download mode
76	GNSS_NRST	DI	1.8 V	Reset input signal of the GNSS chip	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
77, 78	RESERVED	-		Reserved	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
79–82	GND	-		Ground	GND	-	-	Ground	GND	-	-	Ground
83	GRFC1	DO	1.8 V	Generic RF controller	GRFC1 [22]	DO	1.8 V	Generic RF controller	RESERVED	-	-	Reserved
84	GRFC2	DO	1.8 V	Generic RF controller	GRFC2 [22]	DO	1.8 V	Generic RF controller	RESERVED	-	-	Reserved
85	GPIO6	DIO	1.8 V	General-purpose input/output	GPIO6	DIO	1.8 V	General-purpose input/output	RESERVED	-	-	Reserved

[22] BG95-M4 does not support GRFC interfaces (pin 83 and pin 84).

86	GPIO7	DIO	1.8 V	General-purpose input/output	GPIO7	DIO	1.8 V	General-purpose input/output	RESERVED	-	-	Reserved
87	GPIO8	DIO	1.8 V	General-purpose input/output	GPIO8	DIO	1.8 V	General-purpose input/output	RESERVED	-	-	Reserved
88	GPIO9	DIO	1.8 V	General-purpose input/output	GPIO9	DIO	1.8 V	General-purpose input/output	RESERVED	-	-	Reserved
89–91	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground
92, 93	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
94	CLI_RXD	DI	1.8 V	CLI UART receive	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
95	CLI_TXD	DO	1.8 V	CLI UART transmit	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
96	PON_TRIG	DI	1.8 V	Used for main UART function control and for entering/exiting e-I-DRX, PSM, sleep and power off modes	PON_TRIG	DI	1.8 V	Wake up the module from PSM	RESERVED	-	-	Reserved
97	GNSS_EN	DI	1.8 V	Enable internal GNSS chip	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
98	SFNIND_1PPS	DO	1.8 V	One pulse per second	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
99	VDD_RF	PO	1.8 V	Reserved	RESERVED	-	-	Reserved	RESERVED	-	-	Reserved
100–102	GND	-	-	Ground	GND	-	-	Ground	GND	-	-	Ground

NOTE

1. On BG95 series, GNSS_TXD (pin 27), GRFC2 (pin 84) and GNSS_LNA_EN (pin 51) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
2. On BG950A-GL/BG951A-GL/BG95 series/BG96, ADC input voltage must not exceed 1.8 V.
3. Keep all RESERVED and unused pins unconnected.
4. All GND pins should be connected to ground.
5. Pins in **blue** are compatible pins on BG950A-GL, BG951A-GL, BG95 series and BG96 that have different functions.

4 Application Interfaces

The following chapters describe the compatible design between BG950A-GL, BG951A-GL, BG95 series and BG96 on main functionalities.

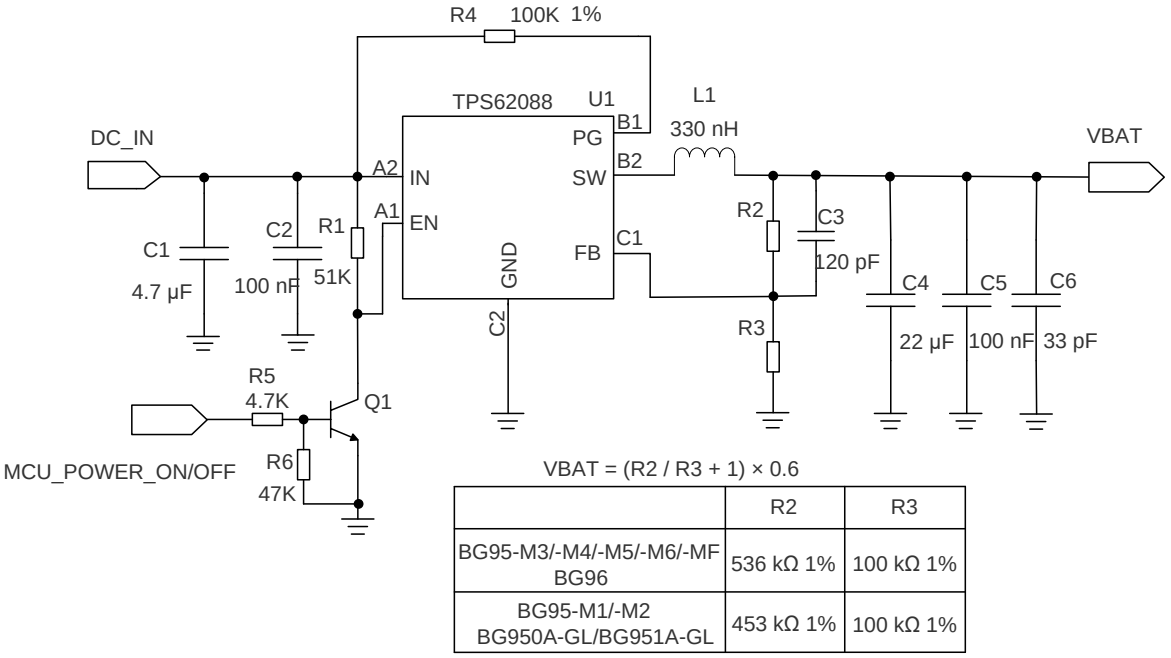
4.1. Power Supply

4.1.1. Reference Design for Power Supply

Power design for a module is critical to its performance. BG950A-GL, BG951A-GL, BG95 series and BG96 modules are LPWA modules which require low quiescent and leakage current. BG95 series and BG96 also support 2G network, therefore, the power IC must be able to provide sufficient current output for 2G network.

If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following is an external power supply reference design of BG950A-GL, BG951A-GL, BG95 series and BG96 modules where buck converter solution is used.



	R2	R3
BG95-M3/-M4/-M5/-M6/-MF BG96	536 kΩ 1%	100 kΩ 1%
BG95-M1/-M2 BG950A-GL/BG951A-GL	453 kΩ 1%	100 kΩ 1%

Figure 2: Reference Design of External Power Supply

Pay attention to the power supply design for BG950A-GL/BG951A-GL/BG95 series/BG96:

- If only LTE Cat M1 and/or Cat NB1 networks are used, it is recommended to select a DC-DC converter chip or an LDO chip with ultra-low leakage current and current output no less than 1.0 A for the power supply.
- If LTE Cat M1, Cat NB1 and EGPRS networks are all used, the current output of DC-DC converter chip or LDO chip cannot be lower than 2.7 A and power supply chips with low leakage current should be selected due to the module needs higher current when transmitting in GSM network.

4.1.2. Voltage Stability Requirements

The power supply range of the modules are listed below:

- **BG950A-GL & BG951A-GL:** 2.2–4.35 V, typ.3.3 V
- **BG95-M1/-M2:** 2.6–4.8 V, typ. 3.3 V
- **BG95-M3/-M5/-M6/-MF:** 3.3–4.3 V, typ. 3.8 V
- **BG95-M4:** 3.2–4.2 V, typ. 3.8 V
- **BG96:** 3.3–4.3 V, typ. 3.8 V

Make sure the input voltage remains at 3.3–4.2 V in the compatible design of BG950A-GL, BG951A-GL, BG95 series and BG96. For all modules involved, the main power supply from an external application must be a single voltage source and can be expanded to two sub paths with star structure (VBAT_BB and VBAT_RF).

In addition, to avoid the damage caused by electric surge and ESD, it is recommended that a TVS diode with low reverse stand-off voltage (V_{RWM}), low leakage current, low clamping voltage (V_C) and high reverse peak pulse current (I_{PP}) should be used.

A power supply reference design for BG950A-GL and BG951A-GL is presented in the following figure.

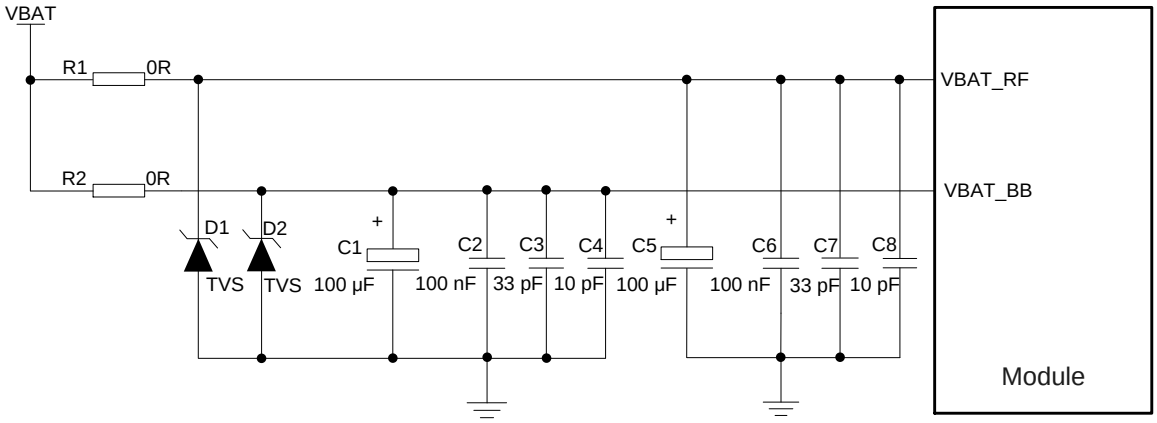


Figure 3: Power Supply in Star-Shaped Pattern (BG950A-GL/BG951A-GL)

A power supply reference design for BG95 series is presented in the following figure.

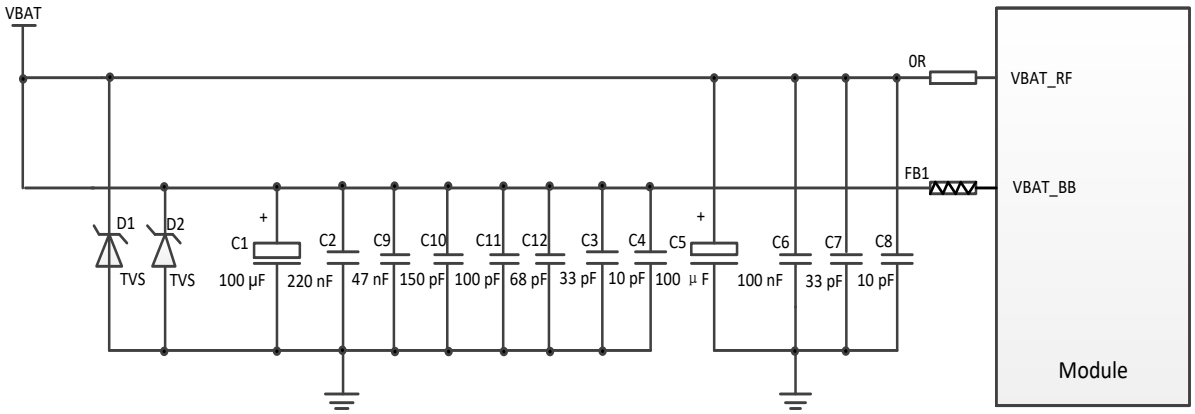


Figure 4: Power Supply in Star-Shaped Pattern (BG95 Series)

A power supply reference design for BG96 is presented in the following figure.

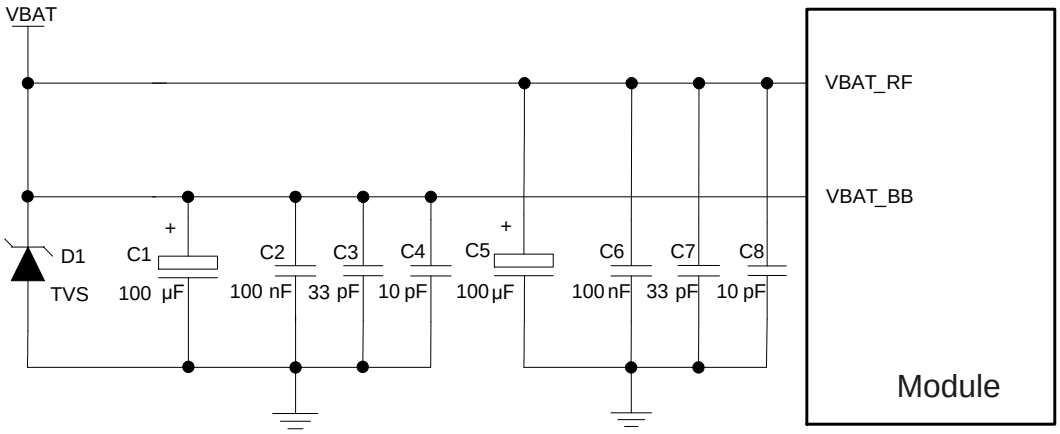


Figure 5: Power Supply in Star-Shaped Pattern (BG96)

4.2. Turn On

BG950A-GL, BG951A-GL, BG95 series and BG96 modules have the same turn-on method.

BG950A-GL/BG951A-GL:

BG950A-GL/BG951A-GL can be turned on by driving PWRKEY low for 500–1000 ms. PWRKEY is pulled up to an internal voltage of the baseband chipset inside the module, and the minimum high-level output voltage is 1.0 V.

BG95 series:

BG95 series can be turned on by driving PWRKEY low for 500–1000 ms. PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.

BG96:

BG96 can be turned on by driving PWRKEY low for at least 500 ms. PWRKEY output voltage is 0.8 V because of the diode drop inside the chipset.

It is recommended to use an open drain/collector driver to control the PWRKEY. A reference design of the turn-on circuit for BG950A-GL, BG951A-GL, BG95 series and BG96 is presented in the following figure.

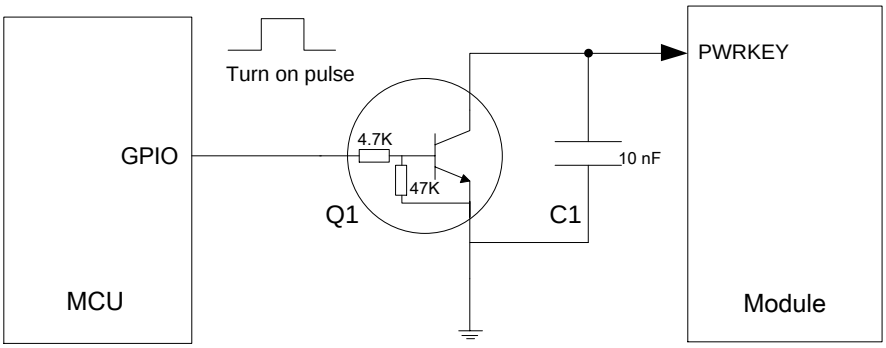


Figure 6: Turn On the Module with a Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from fingers. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference design is illustrated in the following figure.

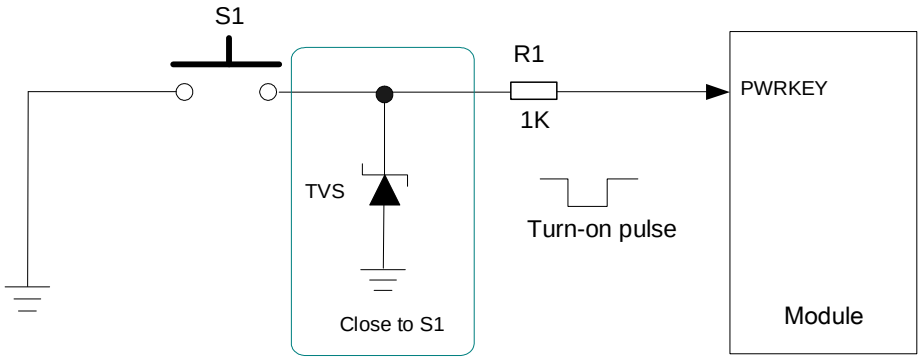


Figure 7: Turn On the Module with Button

BG950A-GL & BG951A-GL:

The power-up timing of BG950A-GL/BG951A-GL varies with the VBAT stable duration before you drive PWRKEY low.

1) Drive PON_TRIG high and then drive PWRKEY low when VBAT is stable for 100–200 ms, BG950A-GL and BG951A-GL will be turned on immediately, and in this case, the power-up timing is shown below.

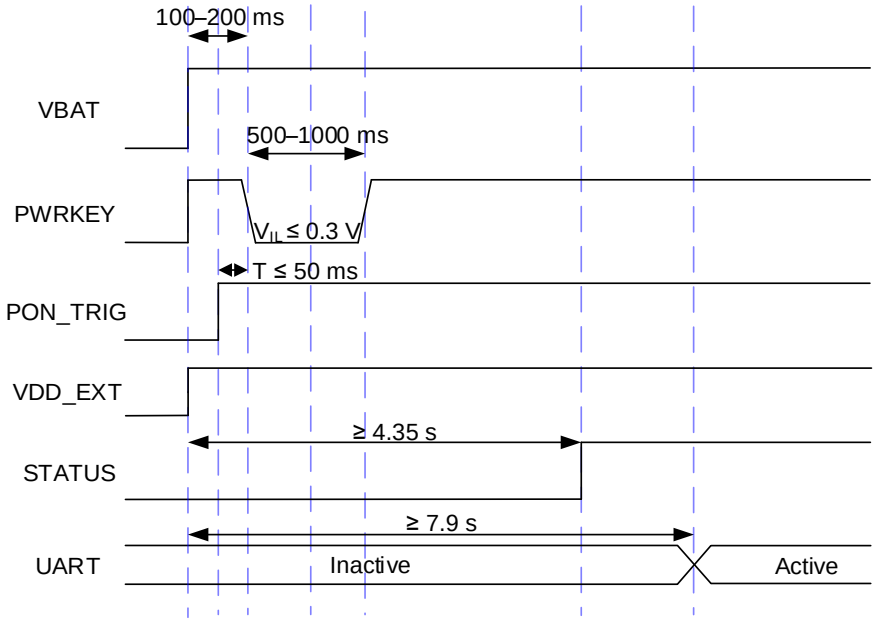


Figure 8: Power-up Timing When VBAT is Stable for 100–200 ms (BG95xA-GL)

2) Drive PON_TRIG high and drive PWRKEY low after VBAT is stable for more than 250 ms, BG950A-GL and BG951A-GL will be turned on immediately, and in this case, the power-up timing is shown below.

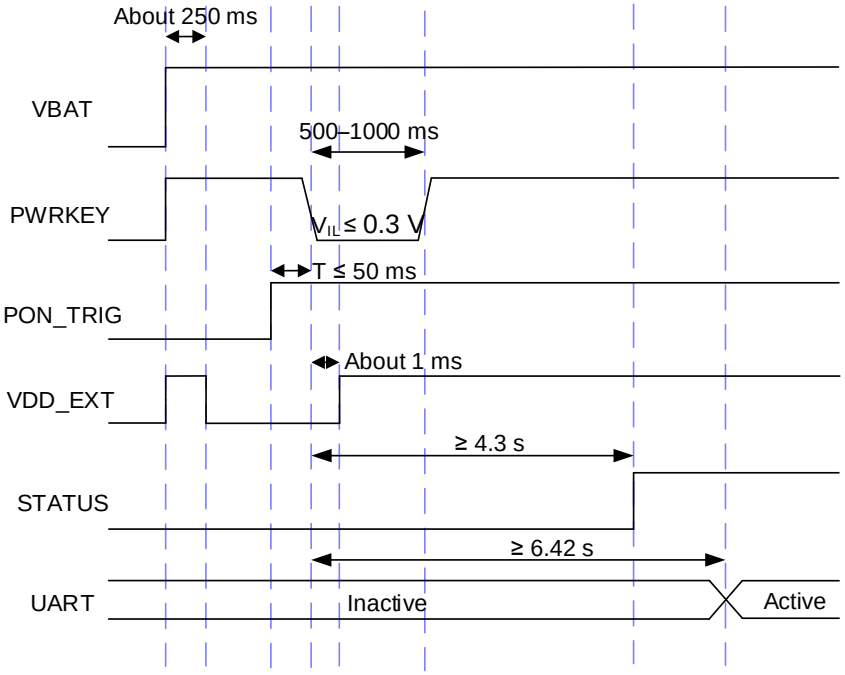


Figure 9: Power-up Timing When VBAT is Stable for More than 250 ms (BG95xA-GL)

After BG950A-GL/BG951A-GL is turned off with the PWRKEY and PON_TRIG solution or the AT command and PON_TRIG solution, VBAT will keep powered on all the time until the main power supply is disconnected. In this case, drive PON_TRIG high and then drive PWRKEY low will restart the module, and the restart timing is shown below.

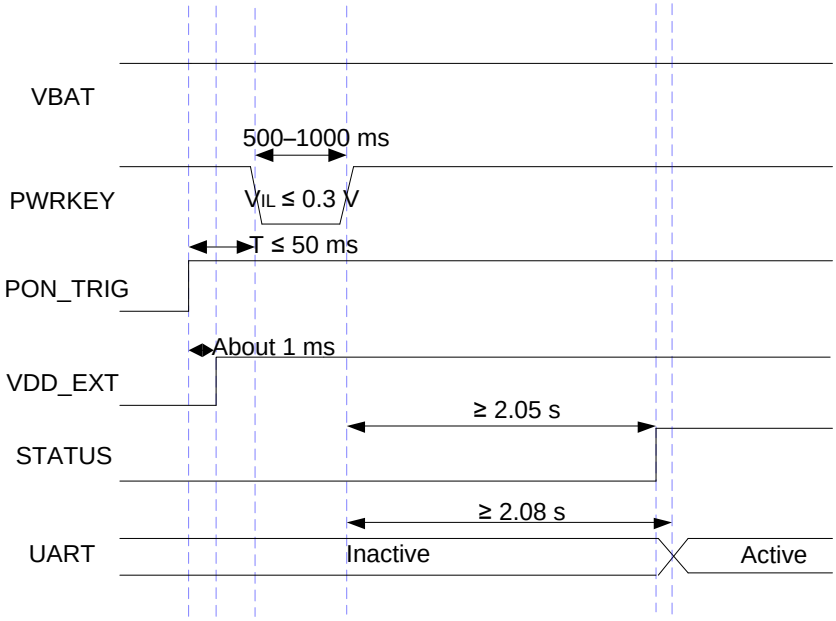


Figure 10: Restart Timing (BG95xA-GL)

NOTE

1. After VBAT is powered on, BG950A-GL/BG951A-GL requires an internal program loading time of about 250 ms.
2. Before you turn on or restart BG950A-GL/BG951A-GL by driving PWRKEY low for 500–1000 ms, drive PON_TRIG high, otherwise, the main UART interface will be inaccessible.

BG95 Series:

The power-up timing of BG95 series is illustrated in the figure below.

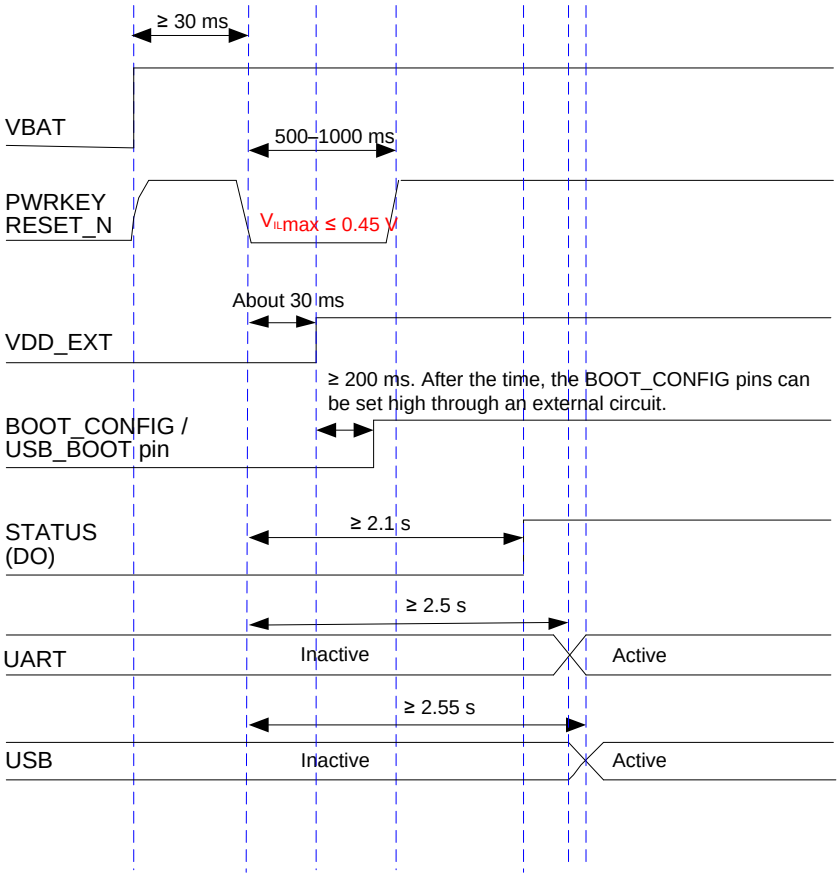


Figure 11: Power-up Timing (BG95 Series)

BG96:

The power-up timing of BG96 is illustrated in the figure below.

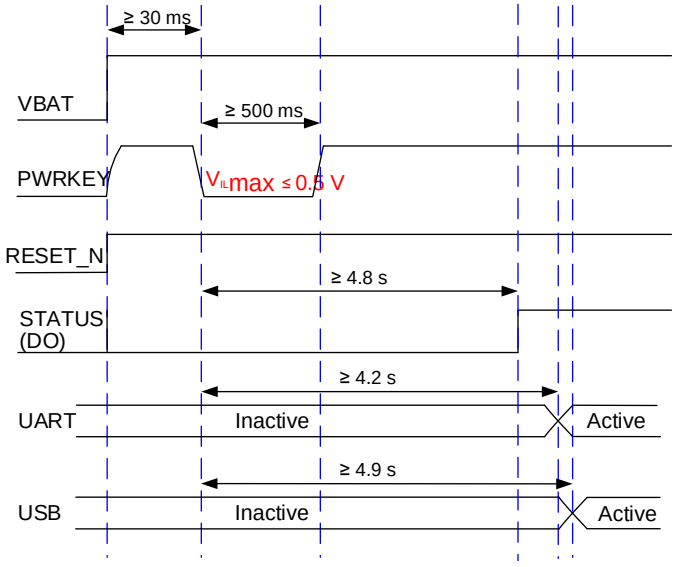


Figure 12: Power-up Timing (BG96)

NOTE

On BG95 series, PWRKEY should never be pulled down to GND permanently.

4.3. Turn Off

4.3.1. Turn Off with PWRKEY

BG950A-GL/BG951A-GL:

When BG950A-GL/BG951A-GL is powered on, drive PWRKEY low for 650–1500 ms and then release it, and then pull down PON_TRIG within 200 ms, after which the module will execute a power-down procedure.

The power-down timing is illustrated in the figure below.

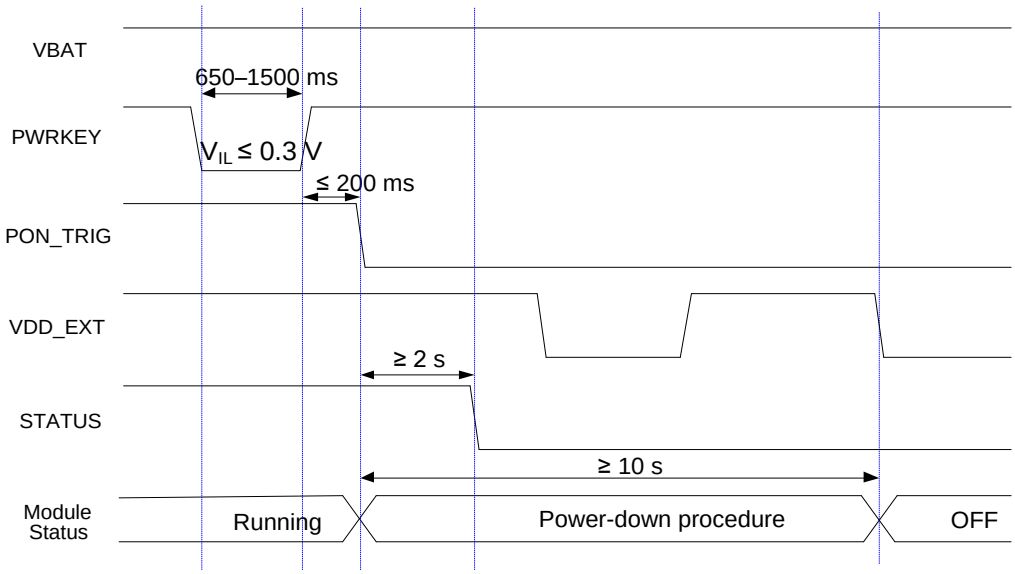


Figure 13: Power-down Timing with PWRKEY & PON_TRIG (BG950A-GL/BG951A-GL)

BG95 Series & BG96:

Driving PWRKEY low (650–1500 ms on BG95 series; at least 650 ms on BG96) and then releasing it, BG95 series and BG96 will execute power-down procedure. In this case, the power-down timing is illustrated in the figure below.

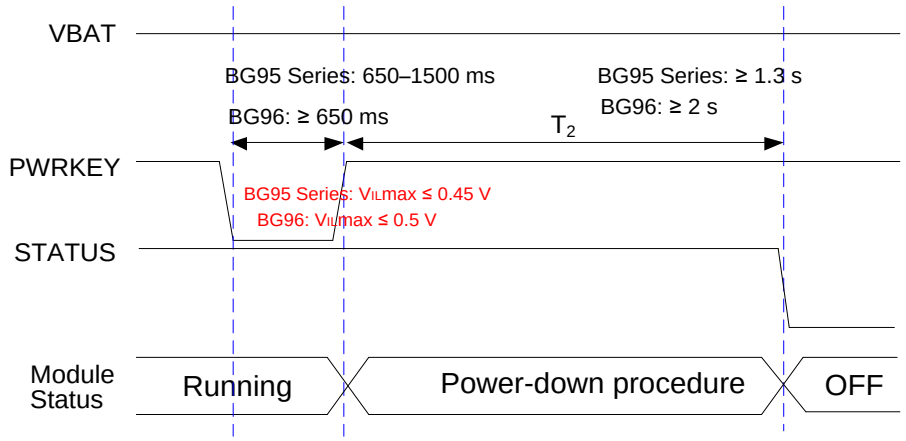


Figure 14: Power-down Timing with PWRKEY (BG95 Series and BG96)

4.3.2. Turn Off with AT Command

There are several ways to turn off BG950A-GL, BG951A-GL, BG95 series and BG96. It is recommended to turn off the modules through **AT+QPOWD**, which is a safe way. It is similar to turning off the module with PWRKEY. The command will make the module log out from the network and save important data via the firmware before completely disconnecting the power supply.

BG950A-GL & BG951A-GL:

After the **AT+QPOWD** is sent, pull down PON_TRIG within 200 ms, and the module will execute the power-down procedure. In this case, the power-down timing is illustrated in the figure below.

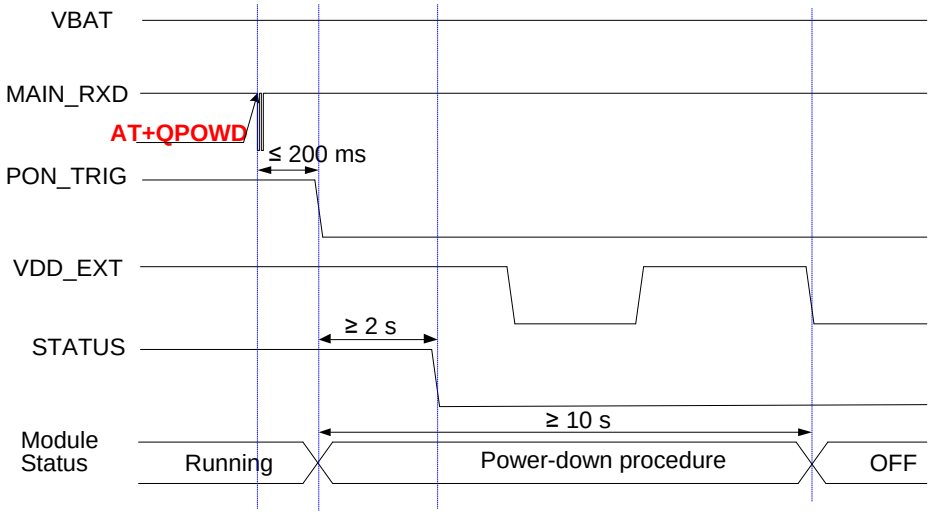


Figure 15: Power-down Timing with AT Command & PON_TRIG (BG950A-GL & BG951A-GL)

BG95 Series & BG96:

The power-down timing of BG95 series and BG96 is illustrated in the figure below.

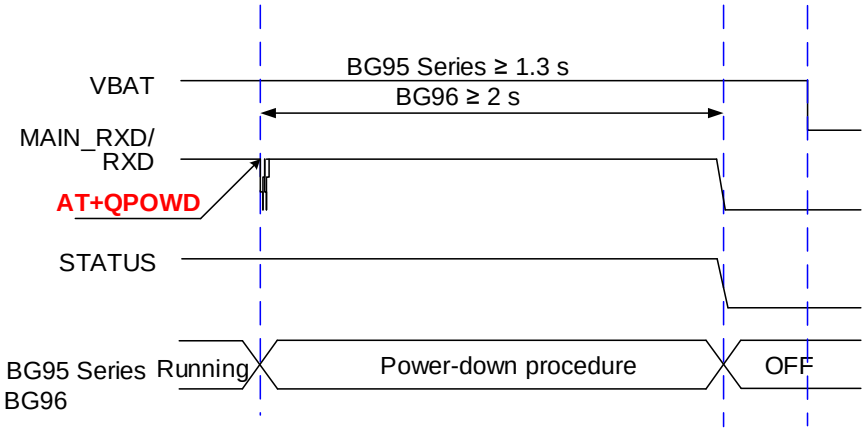


Figure 16: Power-down Timing with AT Command (BG95 Series/BG96)

4.4. Reset

- BG950A-GL and BG951A-GL can be reset by driving RESET_N low for at least 100 ms.
- BG95 series can be reset by driving RESET_N low for 2–3.8 s.
- BG96 can be reset by driving RESET_N low for 150–460 ms.

The recommended circuits for RESET_N are shown below and they are similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N pin.

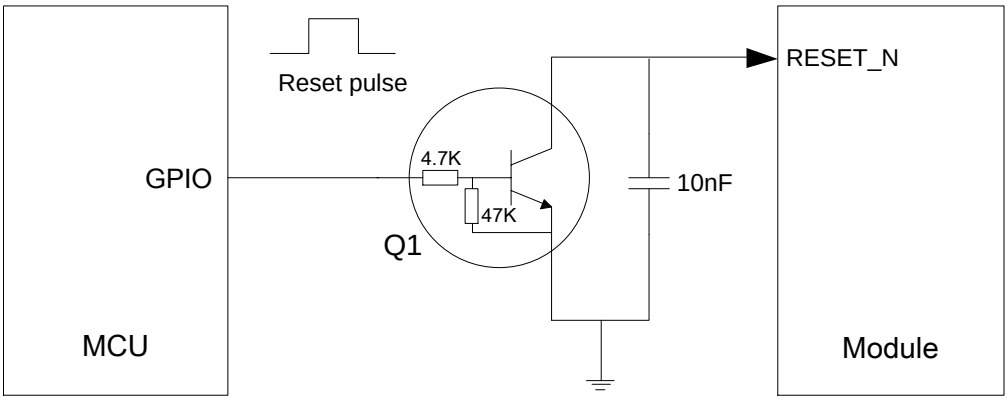


Figure 17: Reference Design of RESET_N with a Driving Circuit

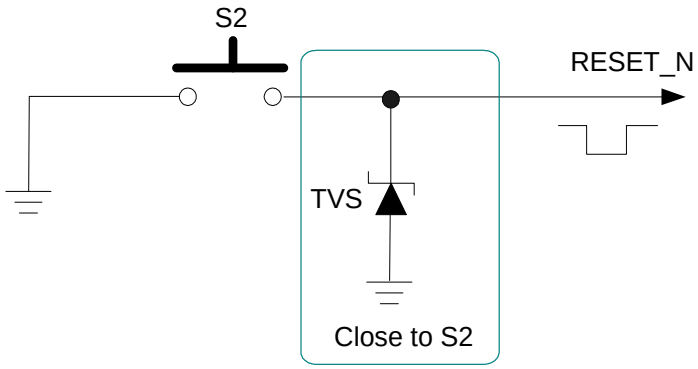


Figure 18: Reference Design of RESET_N with Button

The reset timing of the modules is illustrated in the figure below.

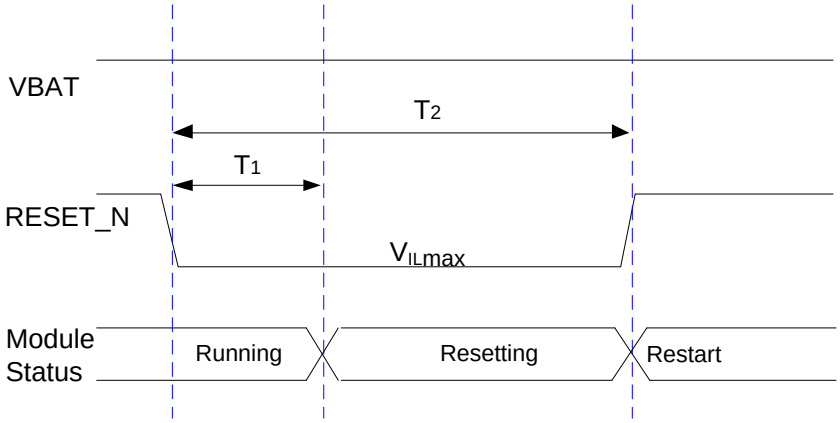


Figure 19: Reset Timing

Table 7: Reset Timing

Module	V_{IL}max	T_1	T_2
BG950A-GL/BG951A-GL	≤ 0.3 V	-	≥ 100 ms
BG95 series	≤ 0.45 V	≥ 2 s	≤ 3.8 s
BG96	≤ 0.5 V	≥ 150 ms	≤ 460 ms

NOTE

1. Use RESET_N only when turning off the module by **AT+QPOWD** and PWRKEY pin both failed.
2. Ensure that there is no large capacitance on and RESET_N.

4.5. PON_TRIG

BG95 series:

PON_TRIG on BG95 series is used to wake up the module from PSM. When the pin detects a rising edge and keeps at high level for at least 30 ms, the module wakes up from PSM.

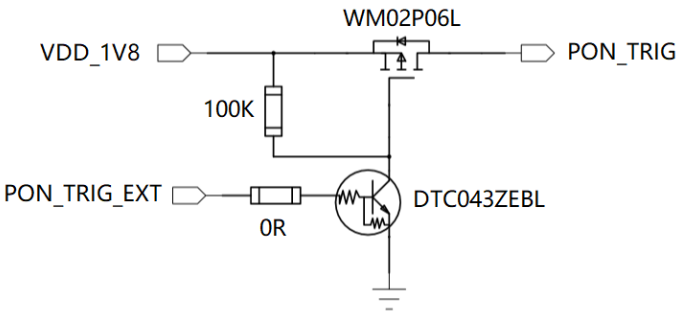


Figure 20: Reference Design of PON_TRIG (BG95 Series)

BG950A-GL/BG951A-GL:

PON_TRIG on BG950A-GL/BG951A-GL can realize the following functions:

- Control the module to enter or exit e-I-DRX, PSM mode and sleep mode.
- Enable/disable the main UART interface communication function.
- Used for the turn-on/off application of the module.

PON_TRIG on BG950A-GL/BG951A-GL must be designed to allow for external control. A reference design is shown in the following figure.

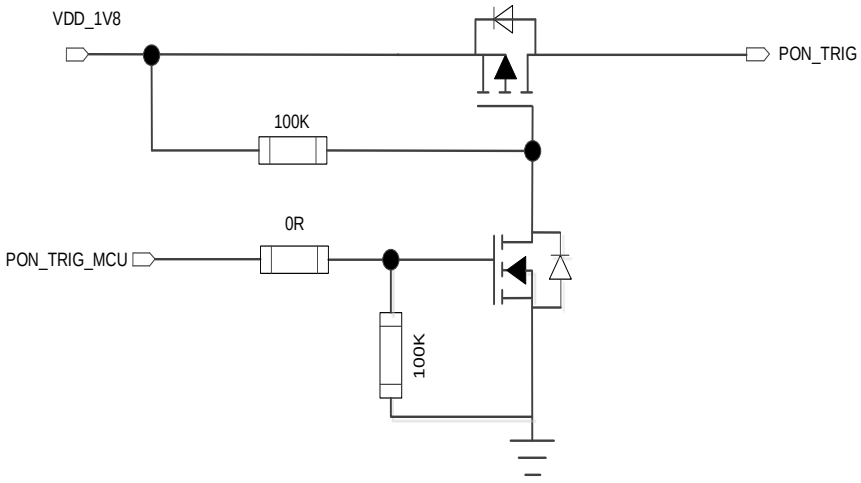


Figure 21: PON_TRIG Reference Design 1 (BG950A-GL/BG951A-GL)

In addition, a voltage divider circuit can be used to control PON_RIG. Pay attention to the voltage domain of the external host and the selection of the voltage divider resistor. A voltage divider circuit in the 3.3 V host voltage domain is shown in the following figure.

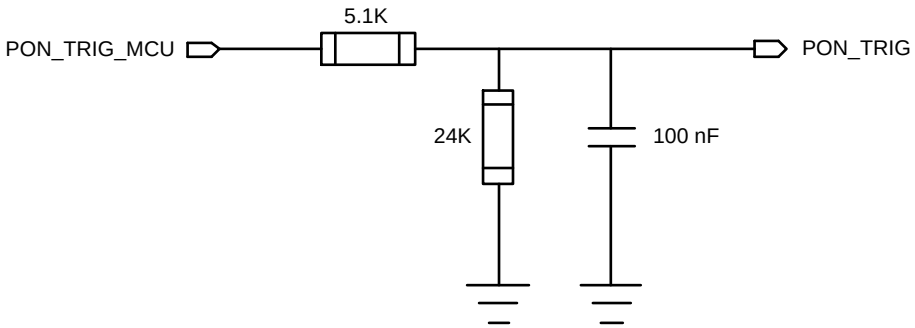


Figure 22: PON_TRIG Reference Design 2 (BG950A-GL/BG951A-GL)

NOTE

1. In ***Figure 20*** and ***Figure 21***, VDD_1V8 is provided by an external LDO.
2. In ***Figure 22***, if the host's voltage domain is not 3.3 V, the value of the voltage divider resistors should be tested according to your actual application.

4.6. (U)SIM Interface

BG950A-GL, BG951A-GL, BG95 series and BG96 support one (U)SIM interface.

- BG96 supports 1.8/3.0 V (U)SIM card.
- BG950A-GL, BG951A-GL and BG95 series only support 1.8 V (U)SIM card.

The following figure shows a reference design for (U)SIM interface with a 6-pin (U)SIM card connector.

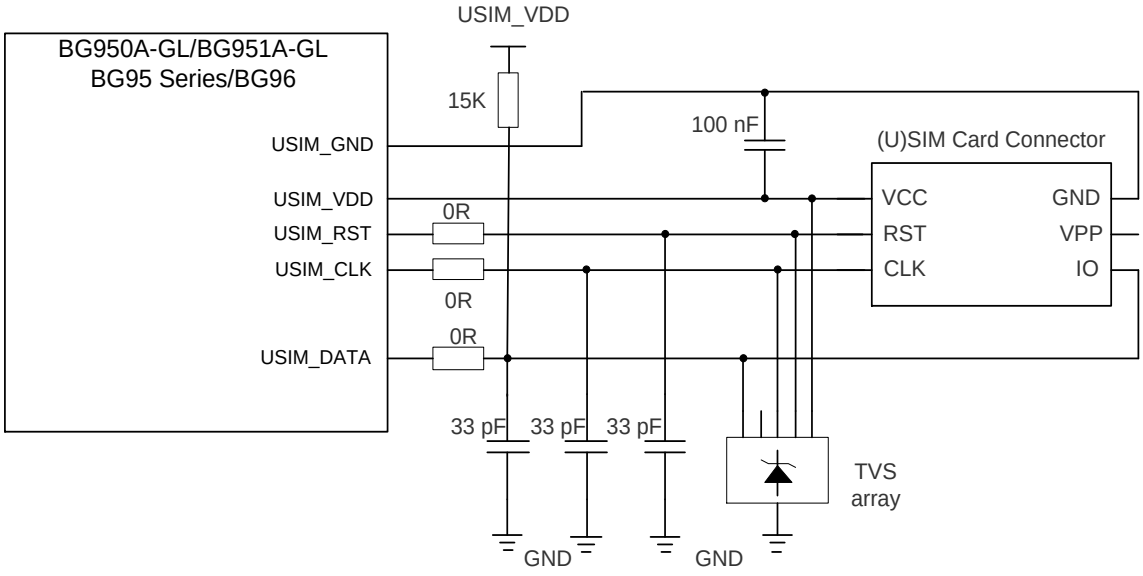


Figure 23: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

If (U)SIM card detection function needs to be used, keep USIM_DET/USIM_PRESENCE connected. The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

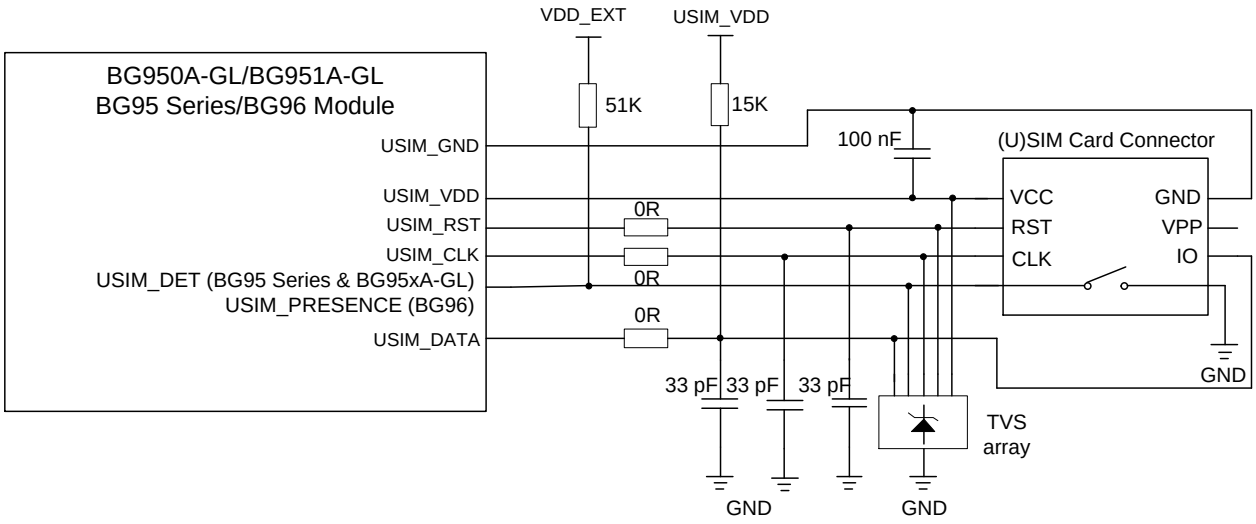


Figure 24: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

4.7. UART Interfaces

BG950A-GL & BG951A-GL:

BG950A-GL provides three UART interfaces: main UART, CLI UART, debug UART interfaces. BG951A-GL provides four UART interfaces: main UART, CLI UART, debug UART and GNSS UART interfaces.

- **Main UART:**
  It supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates, and the default baud rate is 115200 bps. It is used for AT command communication and data transmission, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- **CLI UART:**
  It supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates, and the default baud rate is 115200 bps. It is used for firmware upgrade, software debugging, log output, GNSS data and NMEA sentences output, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- **Debug UART:**
  It supports 921600 bps baud rate by default, and is used for RF calibration and log output, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- **CLI/GNSS UART:**
  On BG950A-GL, pin 27 and pin 28 only function as CLI UART interface (pin 27: CLI_TXD; pin 28: CLI_RXD). In this case, the two pins are connected to pin 95 and pin 94 respectively inside the module. On BG951A-GL, pin 27 and pin 28 only function as GNSS UART interface (pin 27: GNSS_TXD; pin 28: GNSS_RXD) which supports 115200 bps baud rate by default, and is used for GNSS data and NMEA sentences output.

BG95 Series:

BG95 series provides three UART interfaces: main UART, debug UART and GNSS UART interfaces.

- **Main UART:**
  It is used for data transmission and AT command communication, and supports RTS and CTS hardware flow control, and the default baud rate is 115200 bps. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- **Debug UART:**
  It is used for software debugging and log output, and supports a fixed baud rate of 115200 bps.
- **GNSS UART:**
  GNSS UART interfaces are used for GNSS data and NMEA sentence output and the default baud rate is 115200 bps.

BG96:

BG96 provides three UART interfaces: UART1, UART2 and UART3 interfaces.

- **UART1 (main UART):**
  It is used for data transmission and AT command communication, and supports RTS and CTS hardware flow control, and the default baud rate is 115200 bps.
- **UART2 (debug UART):**
  It is used for software debugging, log output, and supports 115200 bps baud rate.
- **UART3 (GNSS UART):**
  It is used for outputting GNSS data, NMEA sentences and supports 115200 bps baud rate.

Since the UART interface power domain of all modules involved is 1.8 V, a voltage-level translator should be used if your application is equipped with a 3.3 V UART interface.

For BG950A-GL and BG951A-GL, it is recommended to use a level-shifting chip without internal pull-up. The voltage-level translator TXB0108PWR provided by *Texas Instruments* is recommended.

For BG95 series and BG96 module, it is recommended to use a level-shifting chip (with or without internal pull up), such as TXS0108EPWR.

Visit http://www.ti.com for more information about the level-shifting chips.

The following figure shows a reference design.

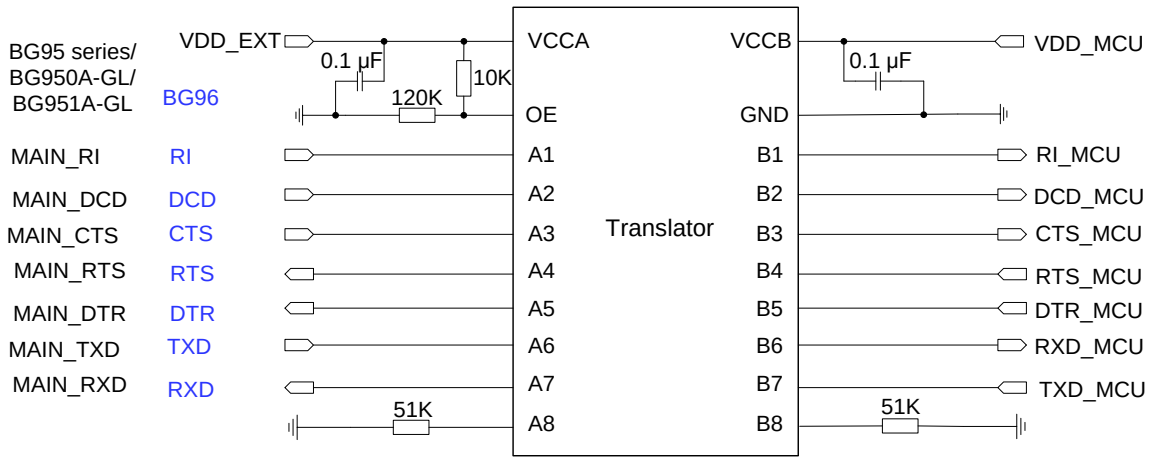


Figure 25: Reference Design with Translator Chip

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

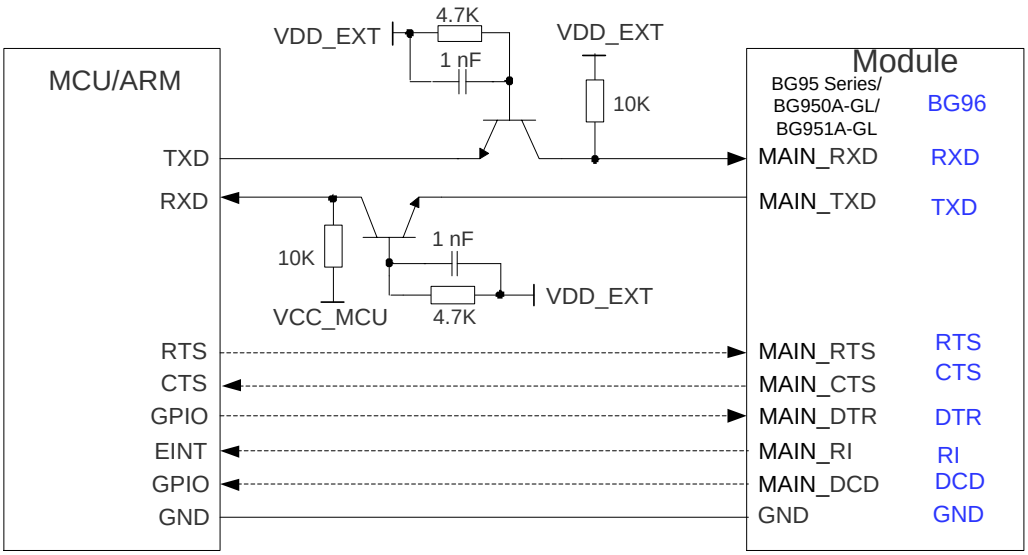


Figure 26: Reference Design with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the host's RTS.

4.8. USB Interface

BG950A-GL, BG951A-GL, BG95 series and BG96 provide one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports slave mode only.

Table 8: Data Rate and Function of USB Interface

Module	Data Rate	Function
BG950A-GL/BG951A-GL	Full speed (12 Mbps)	● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade
BG95 series	High speed (480 Mbps) Full speed (12 Mbps) Low speed (1.5 Mbps)	● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade ● GNSS NMEA sentences output

BG96	High speed (480 Mbps) Full speed (12 Mbps)	● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade

The following figure shows a reference design of USB interface for BG950A-GL/BG951A-GL/BG95 series.

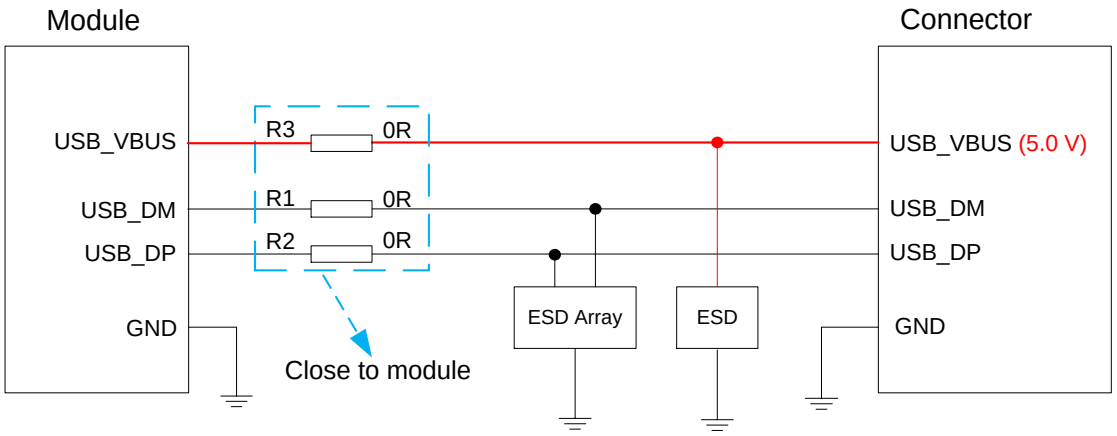


Figure 27: Reference Design of USB Interface (BG950A-GL/BG951A-GL/BG95 Series)

The following figure shows a reference design of USB interface for BG96.

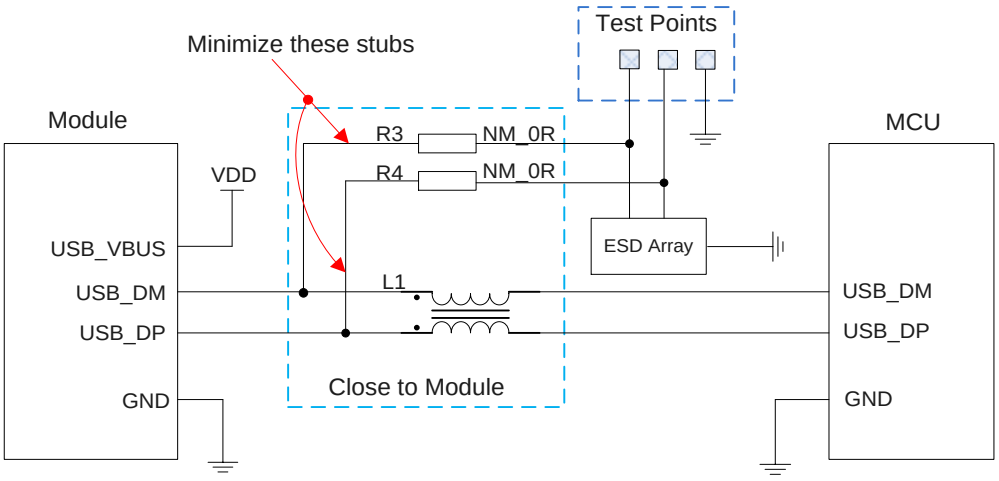


Figure 28: Reference Design of USB Interface (BG96)

For more details about the USB interface of all modules involved, see ***document [1]*** and ***document [2]*** and ***document [3]***.

NOTE

1. BG950A-GL, BG951A-GL, BG95 series and BG96 can only be used as a slave device.
2. In practical applications, the constant use of USB will increase power consumption. Therefore, in power-sensitive applications, it is recommended that USB interface is used for firmware upgrade only.

4.9. PCM and I2C Interfaces

BG950A-GL and BG951A-GL do not support PCM and I2C interfaces.

BG95 series and BG96 provide one Pulse Code Modulation (PCM) digital interface and one I2C interface. A reference design of PCM and I2C interfaces with an external codec IC is shown below.

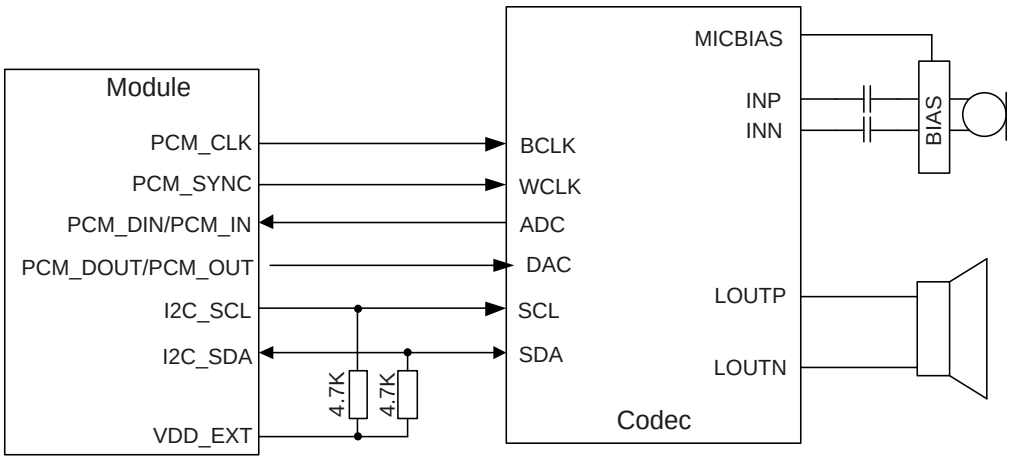


Figure 29: Reference Design of PCM Application with Audio Codec (BG95 Series & BG96)

4.10. ADC Interfaces

BG950A-GL, BG951A-GL, BG95 series and BG96 provide two analog-to-digital converter (ADC) interfaces.

On BG95 series, ADC0 and ADC1 cannot be used simultaneously, as ADC1 connects directly to ADC0 inside the module. If the two ADC interfaces of BG95 series are intended to be used at the same time, please add an external analog switch.

For BG950A-GL, BG951A-GL and BG96, **AT+QADC=0** can be used to read the voltage value on ADC0

pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. For more details about the AT command, see ***document [4]*** and ***document [6]***.

For BG95 series, **AT+QADC=0** can be used to read the voltage value on the ADC being used. For more details about the AT command, see ***document [5]***.

For more details about the ADC interfaces of all modules involved, see ***document [1]*** and ***document [2]*** and ***document [3]***.

NOTE

1. ADC input voltage must not exceed 1.8 V.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1 %.

4.11. GPIO Interfaces

BG950A-GL, BG951A-GL, BG95 series and BG96 provide general-purpose input and output (GPIO) interfaces.

BG950A-GL, BG951A-GL and BG95 series provide nine general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** can be used to configure the status of corresponding GPIO pins. For more details about the AT command, see ***document [4]*** and ***document [5]***.

For BG96, the module provides two general-purpose input and output (GPIO) interfaces. **AT+QCFG="GPIO"** can be used to configure corresponding GPIO pin's status. For more details about the AT command, see ***document [6]***.

For more details about the GPIO interfaces of all modules involved, see ***document [1]*** and ***document [2]*** and ***document [3]***.

NOTE

BG95-MF does not support GPIO3 and GPIO4.

4.12. GRFC Interface

Compared with BG96 module, BG950A-GL, BG951A-GL and BG95 series additionally provide two general RF control interfaces for controlling external antenna tuners.

For more details about the GRFC interface of BG950A-GL, BG951A-GL and BG95 series, see ***document [1]*** and ***document [2]***.

NOTE

1. GRFC2 (pin 84) of BG95 series is a BOOT_CONFIG pin. Never pull it up before startup, otherwise the module cannot power on normally.
2. BG95-M4 does not support GRFC interface.

4.13. RF Antenna Interfaces

BG950A-GL, BG951A-GL, BG95 series and BG96 have two RF antenna interfaces: ANT_MAIN and ANT_GNSS. The impedance of antenna ports is 50 Ω.

To achieve better RF performance, a π-type matching circuit is recommended to be reserved, and the π-type matching components (R1, C1 and C2) should be placed as close the antenna as possible. By default, R1 is 0 Ω, while C1 and C2 are not mounted.

A reference design of the main antenna interface for all modules involved is shown below.

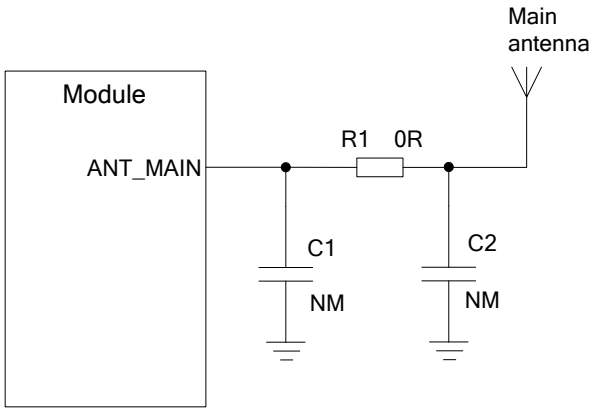


Figure 30: Reference Design of Main Antenna Interface

Reference designs of GNSS antenna interface are shown as below.

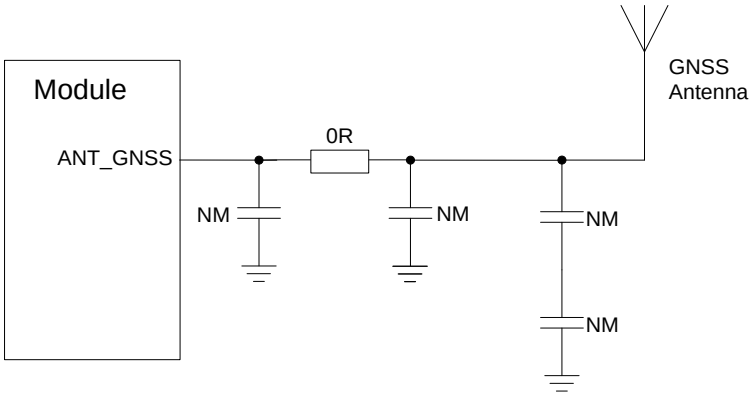


Figure 31: Reference Design of ANT_GNSS Interface (BG950A-GL & BG951A-GL)

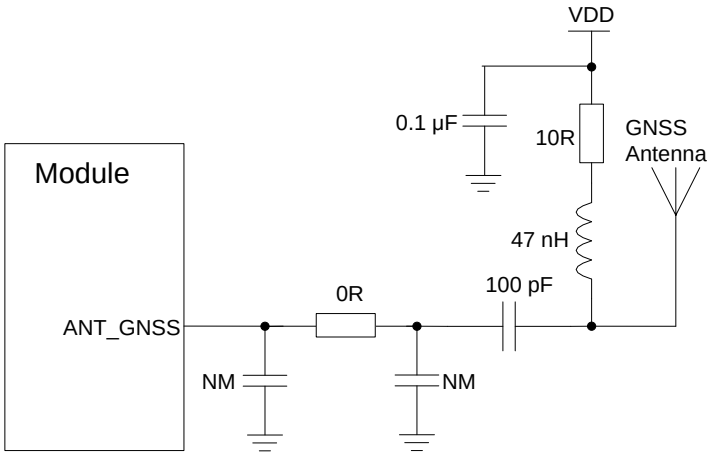


Figure 32: Reference Design of GNSS Antenna Interface (BG95 Series & BG96)

NOTE

1. BG950A-GL/BG951A-GL is designed with a built-in LNA, and supports passive GNSS antenna only. Active antenna and external LNA are not supported.
2. For BG95 series and BG96, an external LDO can be selected to supply power according to the active antenna requirement, and if a passive antenna is selected, then the VDD circuit is not needed.

4.14. Compatible Design Notices

This chapter focuses on the compatible designs to be aware of when migrating from BG95 series/BG96 to BG950A-GL/BG951A-GL.

- **PON_TRIG**

On BG95 series, PON_TRIG is used to wake up the module from PSM. BG96 does not have this pin. On BG950A-GL and BG951A-GL, PON_TRIG is used for main UART function control, turn-on/off application, and entering/exiting e-I-DRX, PSM and sleep modes. Therefore, PON_TRIG pin must be controlled by MCU when migrating from BG95 series/BG96 to BG950A-GL/BG951A-GL, otherwise the module may not be used normally. See ***Chapter 4.5*** for more details.

- **Power supply**

On BG95 series and BG96, pin 32 (VBAT_BB) and pin 33 (VBAT_BB) are used to power the baseband part, and pin 52 (VBAT_RF) and pin 53 (VBAT_RF) are used to power the RF part. While on BG950A-GL/BG951A-GL, pin 32 (VBAT_BB) is used to power the baseband part, pin 33 (VBAT_RF) is used to power the RF part, pin 52 and pin 53 are RESERVED. Therefore, in the power supply compatible design between BG950A-GL, BG951A-GL, BG95 series and BG96, it is necessary to ensure that VBAT_BB and VBAT_RF are routed in star-structure.

- **Test points to be reserved for firmware update and log output**

On BG950A-GL and BG951A-GL, pin 25 (GPIO1), pin 26 (GPIO2) [23], pin 94 (CLI_RXD), pin 95 (CLI_TXD) are used for firmware update and log output. While on BG95 series and BG96, pin 8 (USB_VBUS), pin 9 (USB_DP), pin 10 (USB_DM) are used for firmware update, and pin 22 (DBG_RXD), pin 23 (DBG_TXD) are used for log output. It is recommended to reserve test points for all these pins involved in firmware update or log output. When migrating from BG95 series/BG96 to BG950A-GL/BG951A-GL, pay attention to the difference of pins involved.

- **Emergency download mode**

On BG95 series and BG96, pin 75 (USB_BOOT) is used to force the module into download mode. On BG950A-GL, pin 75 is RESERVED, while on BG951A-GL module, pin 75 (GNSS_BOOT) is used to force the GNSS chip inside the module to enter forced download mode. When migrating from BG95 series/BG96 to BG950A-GL/BG951A-GL, reserve at least one test point for this function.

- **GNSS**

BG95 and BG950A-GL do not support concurrent operation of WWAN and GNSS, while BG96 and BG951A-GL do.

[23] On BG950A-GL and BG951A-GL, pin 25 functions as CLI_RTS and pin 26 functions as CLI_CTS in recovery mode. In other modes, pin 25 and pin 26 are GPIO pins.

BG951A-GL supports GNSS_BOOT (pin 75), GNSS_NRST (pin 76), GNSS_EN (pin 97) and SFNIND_1PPS (pin 98), so pay attention to the design and use of these pins [24] in the BG95 series and BG951A-GL compatible design.

[24] These pins (pins 75, 76, 97 and 98) are all reserved on BG96 and BG950A-GL.

5 Recommended Footprint

This chapter mainly introduces the recommended footprint and stencil design for BG950A-GL, BG951A-GL, BG95 series and BG96 modules. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

5.1. Recommended Compatible Footprint

The following figure shows the bottom views of BG950A-GL, BG951A-GL, BG95 series and BG96 modules.

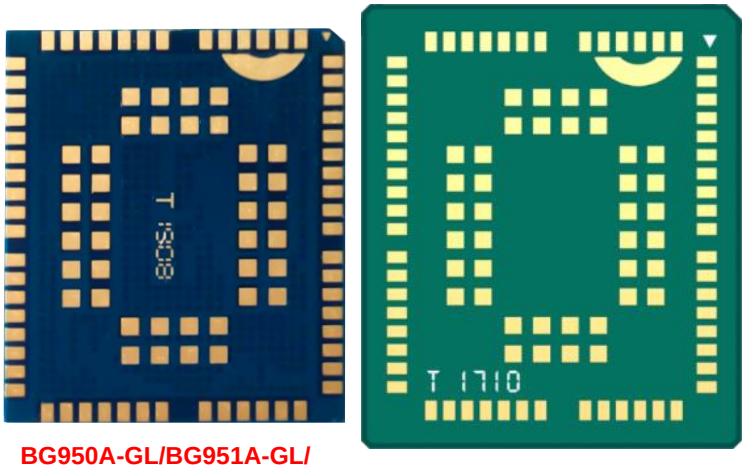


Figure 33: Bottom Views of BG950A-GL/BG951A-GL/BG95 Series/BG96

The following figure shows the recommended compatible footprint of BG950A-GL, BG951A-GL, BG95 series and BG96.

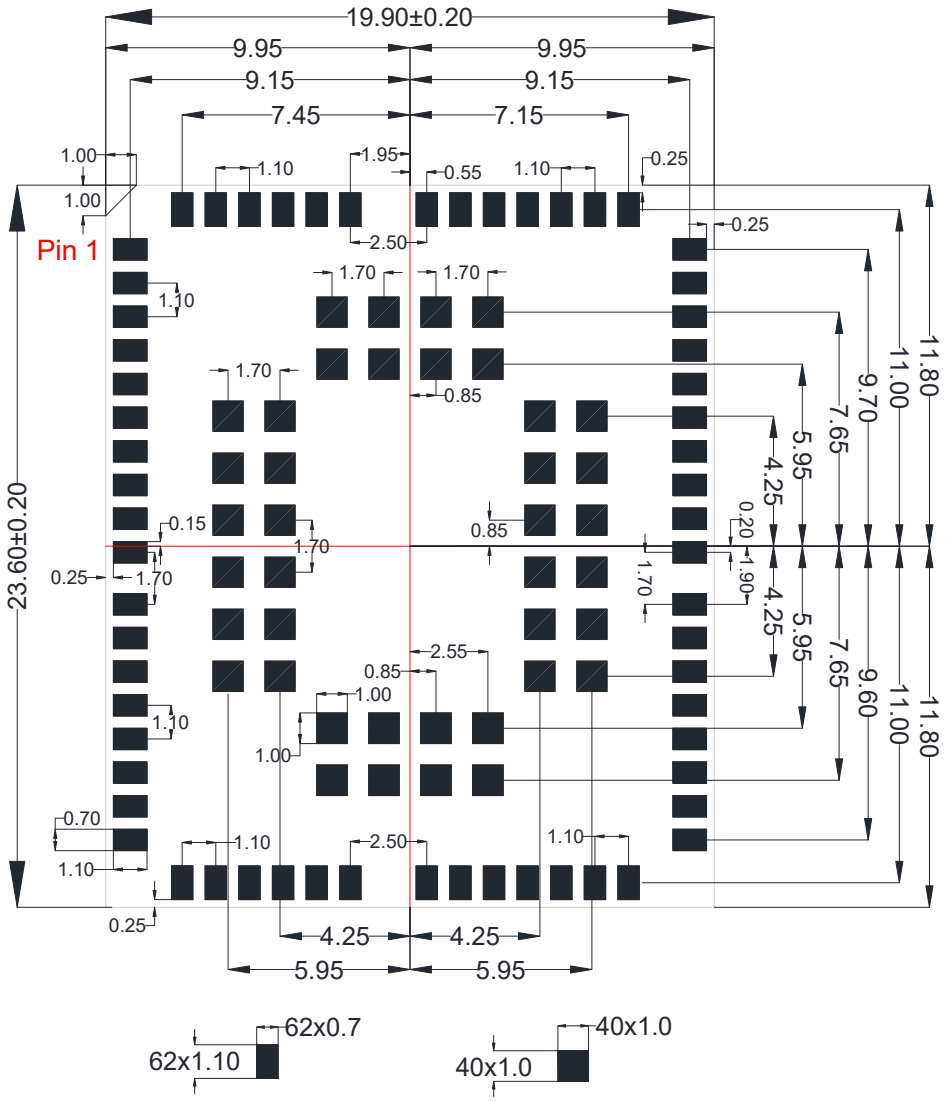


Figure 34: Recommended Compatible Footprint (Top View)

5.2. Installation Sketch Map

The following figure shows the sketch map of installation for BG950A-GL, BG951A-GL, BG95 series and BG96.

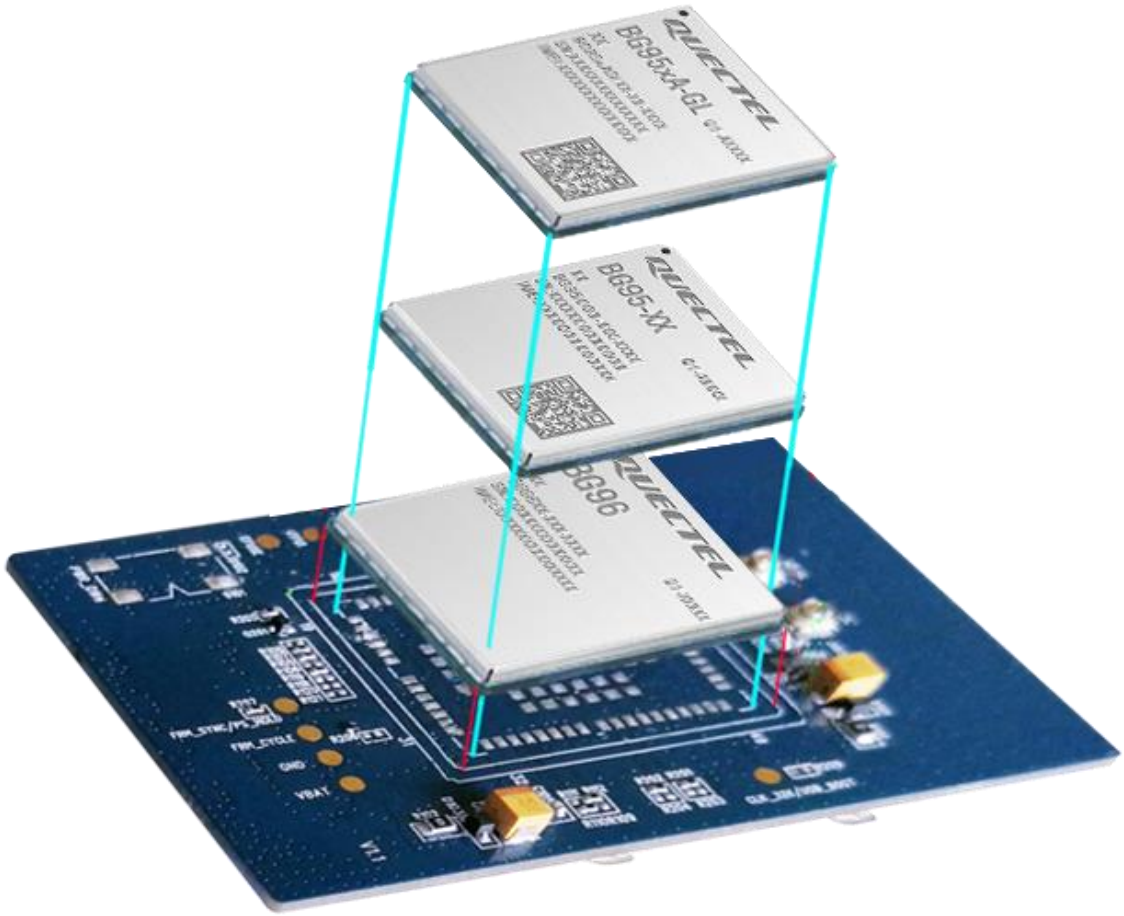


Figure 35: Installation Sketch Map of BG950A-GL/BG951A-GL/BG95 Series/BG96

6 Appendix References

Table 9: Related Documents

Document Name
[1] Quectel_BG950A-GL&BG951A-GL_Hardware_Design
[2] Quectel_BG95_Series_Hardware_Design
[3] Quectel_BG96_Hardware_Design
[4] Quectel_BG77xA-GL&BG95xA-GL_AT_Commands_Manual
[5] Quectel_BG95&BG77&BG600L_Series_AT_Commands_Manual
[6] Quectel_BG96_AT_Commands_Manual

Table 10: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
CLI	Command Line Interface
CS	Circuit Switched
CTS	Clear To Send
DCE	Data Communications Equipment
DFOTA	Delta Firmware upgrade Over-The-Air
DL	Down Link
DRX	Discontinuous Reception
DTE	Data Terminal Equipment

DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EGPRS	Enhanced GPRS
e-I-DRX	Extended Idle Mode Discontinuous Reception
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GRFC	General RF Control
GSM	Global System for Mobile Communications
HD	Half duplex
HSPA	High Speed Packet Access
I2C	Inter-Integrated Circuit
IoT	Internet of Things
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPWA	Low Power Wide Area
LTE	Long Term Evolution
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PCB	Printed Circuit Board

PCM	Pulse Code Modulation
PSM	Power Saving Mode
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RTS	Request To Send
SISO	Single Input Single Output
SMS	Short Message Service
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
UL	Up Link
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VoLTE	Voice over LTE